

Progress Report: Streaming readout for EIC detectors

Jan C. Bernauer
for the eRD23 EIC Streaming Readout Consortium

EIC R&D meeting, BNL January 2019



RBRC
RIKEN BNL Research Center



Stony Brook
University

Who are we: SRC members

- **Catholic University of America:** S. Ali, V. Berdnikov, T. Horn, M. Muhoza, I. Pegg, R. Trotta
- **INFN Genova:** **M. Battaglieri**, A. Celentano
- **Stony Brook University / RBRC:** **J. C. Bernauer**
- **Massachusetts Institute of Technology:** D. K. Hasell, R. Milner
- **Thomas Jefferson National Accelerator Facility:** C. Cuevas, M. Diefenthaler, R. Ent, G. Heyes, B. Raydo, R. Yoshida

Additionally many regulars like Martin Purschke (BNL), Marco Locatelli (CAEN), Jin Huang (BNL), Esko Mikkola (Alphacore),

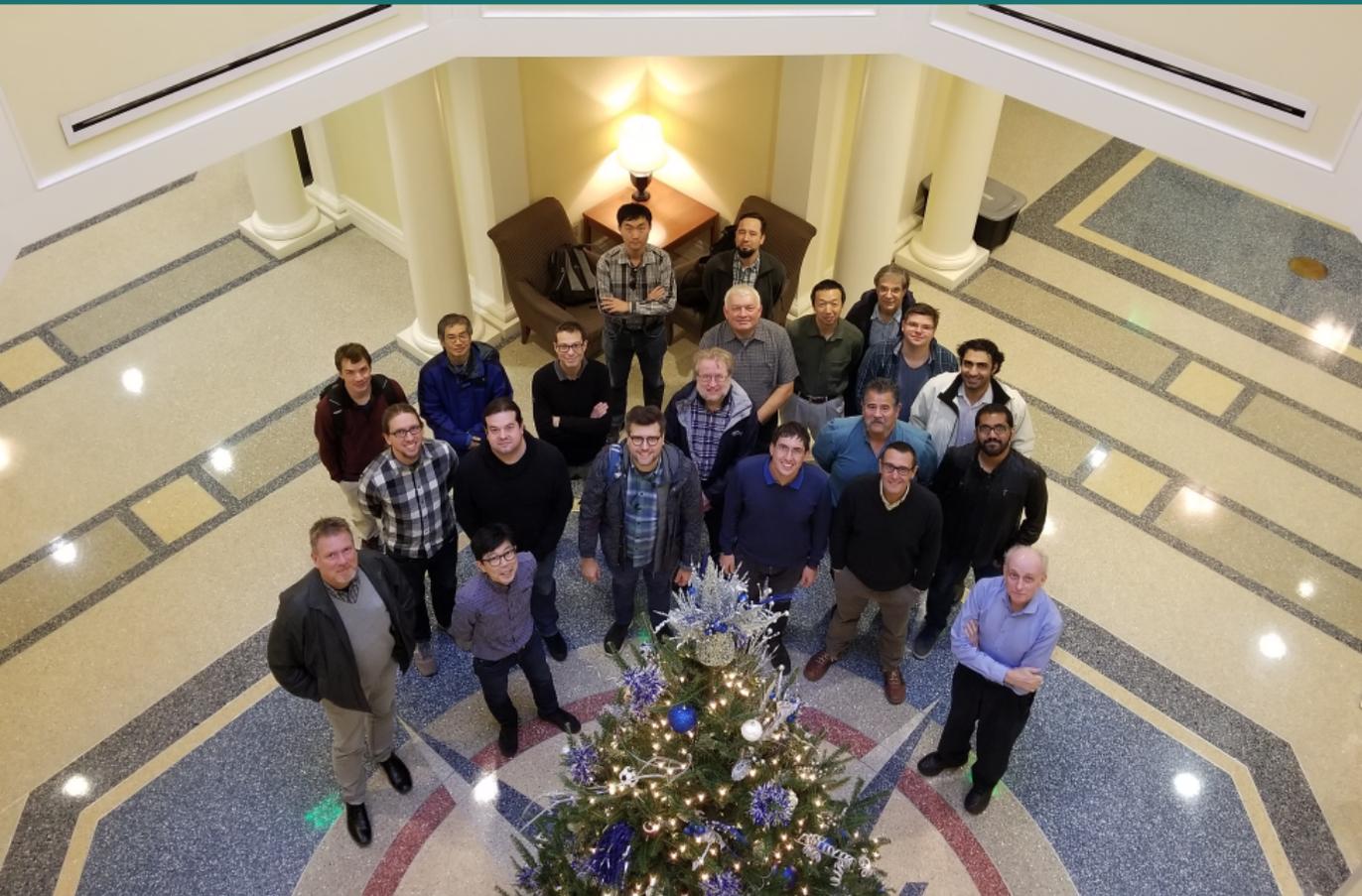
—→ **We welcome new members!** ←—

- Find a readout concept for EIC
- Maximize benefits from streaming readout
- Aim to gain experience with this new paradigm of data read out
- Provide a common platform to develop SRO components

The committee recommends limited travel support for the proponents to further develop the proposal. The proponents are asked to compare streaming solutions with a well-designed conventional triggered system and show where a conventional trigger fails but a streaming readout is plausible.

In accordance with the Committee's priorities and recommendations \$7,500 are awarded to eRD23 for FY19.

December meeting @ CNU



Agenda of December meeting @ CNU

	Monday, 3 December 2018	Tuesday, 4 December 2018
AM	<p>09:00 Welcome (until 10:00)</p> <p>09:00 Welcome</p> <p>09:15 Status of EIC Streaming Readout Initiative - Douglas Hasell (M.I.T.) Slides </p> <p>09:45 Discussion</p> <p>10:00 Data control and validation - Marco Battaglieri (INFN-GE) (until 12:00)</p> <p>10:00 CBM streaming readout DAQ and validation - Volker Friese (GSI) Slides </p> <p>10:30 BDX triggerless DAQ and validation - Andrea Celentano (INFN-Genova) Slides </p> <p>11:00 Discussion Slides </p> <p>12:00 --- Lunch break (on your own) ---</p>	<p>09:00 INDRA tour at Jefferson Lab - David Abbott (Jefferson Lab) Graham Hayes (Jefferson Lab) (until 10:00) (F110 (Turn right at cafe, through glass doors continue ahead past elevators).)</p> <p>10:00 Streaming Readout Software - Markus Diefenthaler (Jefferson Lab) (until 12:00) (L102)</p> <p>10:00 TRIGGERLES Data acqUISition (TRIDAS) for the KM3NET experiment - Tommaso Chiarusi (Istituto Nazionale Fisica Nucleare - Sezione di Bologna) Slides </p> <p>10:30 Software aspects of streaming readout - Markus Diefenthaler (Jefferson Lab) Slides </p> <p>11:00 Discussion</p> <p>12:00 --- Lunch break and return to CNU ---</p>
PM	<p>14:00 Electronics, timing and synchronization - Chris Cuevas (Thomas Jefferson National Accelerator Facility) (until 18:00) Minutes </p> <p>14:00 Streaming Electronics - Benjamin Raydo (Jefferson Lab) Slides </p> <p>14:30 The BDX wave board - Fabrizio Ameli (Sapienza University of Rome) Slides </p> <p>15:00 Status of the JLAB Streaming Data Acquisition Test Stand - Edward Jastrzebski (Jefferson Lab) Slides </p> <p>15:30 Streaming Readout and Timing - William Gu (Jefferson Lab) Slides </p> <p>16:00 Alphacore - Multi-Channel Readout ICs Development Status - Phaneendra Bikkina (Alphacore, Inc.) Daniel Mazidi (Alphacore, Inc.) Slides </p> <p>16:30 Design Study for a sPHENIX based EIC Detector - Progress on streaming demonstrations for EIC - Jin Huang (Brookhaven National Lab) Slides </p> <p>17:00 Discussion</p> <p>18:00 --- Dinner (on your own) ---</p>	<p>14:00 Intermediate network and streaming data - Jan Bernauer (Stony Brook University / RBRC) (until 16:00)</p> <p>14:00 Intermediate network and MPEG presentation Layer - Jan Bernauer (Stony Brook University / RBRC) Minutes Slides </p> <p>14:45 ProIO - David Blyth (Argonne National Laboratory) Slides </p> <p>15:15 Discussion</p> <p>16:00 Closing - Marco Battaglieri (INFN-GE) Jan Bernauer (Stony Brook University / RBRC) (until 17:00)</p>

Data Rates

- Raw data event size: 100 kB / min. bias event (Au+Au)
- At 10 MHz event rate: raw data rate 1 TB/s

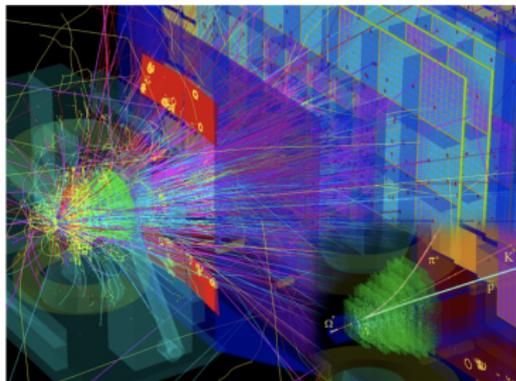
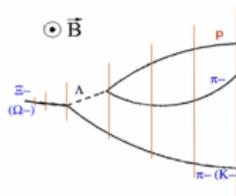
- Archival rate:
 - technologically possible are rates of 100 GB/s and above
 - limiting factor are the storage costs
 - typical runtime scenario 2 effective months / year (5×10^6 s)
 - At 1 GB/s: gives a storage volume of 5 PB/year



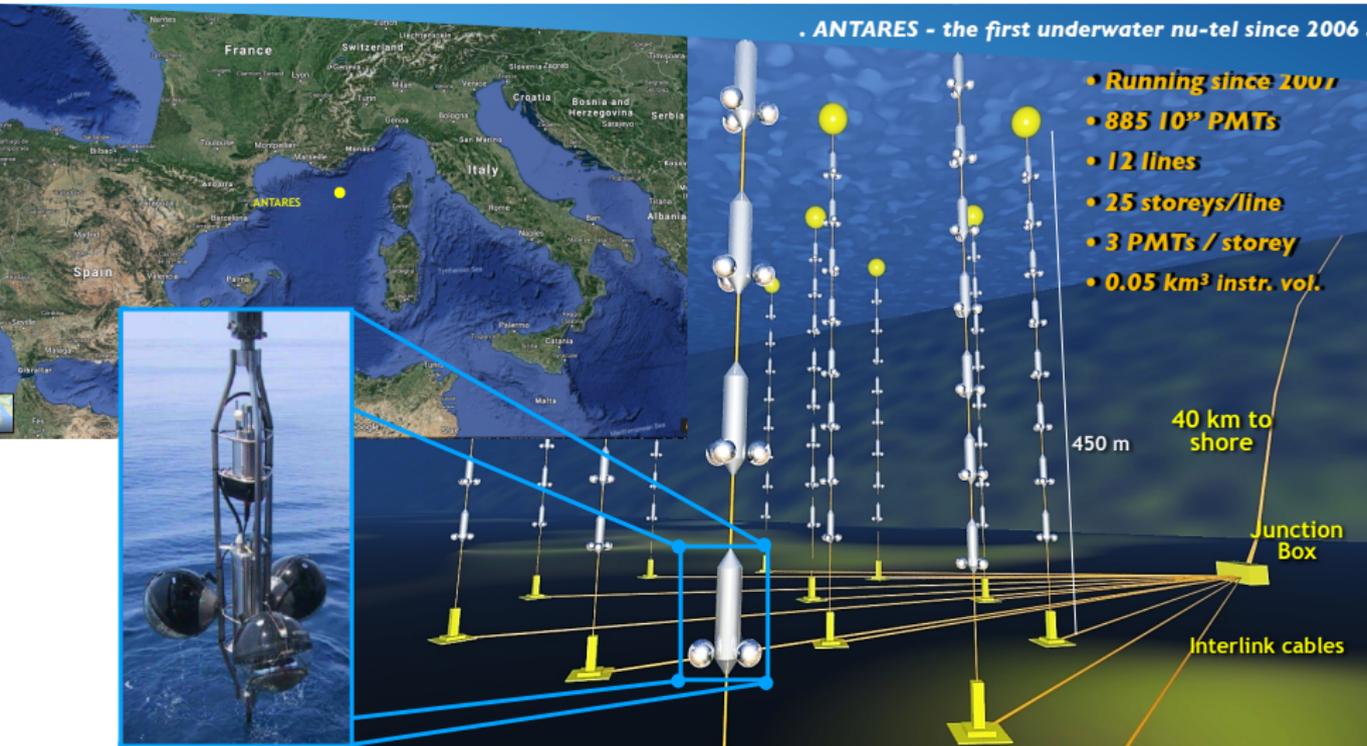
We aim at an data archival rate of a few GB/s, meaning that the raw data volume has to be suppressed online by factors 300 - 1000.

Selecting Data Online

- Some (not all) of the rare probes have a complex signature.
Example: $\Omega \rightarrow \Lambda K^+ \rightarrow p\pi^- K^+$
- In the background of several hundreds of charged tracks
- No simple primitive to be implemented in trigger logic



TRIDAS/KM3net (T. Chiarusi)



The BDX DAQ system: requirements

Number of channels and rates (results obtained from small-scale prototype characterization):

- 1000 CsI(Tl) crystals, each read by a SiPM. Signal rate: 5 Hz/crystal
- 100 active veto channels, each read by a SiPM. Signal rate: 30 Hz/counter

Background rejection requirements:

Whenever there is a EM shower the ECAL, all hits from all veto channels in a $O(10 \text{ us})$ window before and after must be acquired to identify and reject backgrounds, including rare events as muon decays, delayed neutron hits, ...

- First phase “learning”: save all hits (waveforms) to disk. Perform offline analysis to find correlations and define events
- Second phase “production”: implement event selection algorithms in the online software

BDX DAQ system validation

“Physical validation” process:

Compare between “standard” (triggered) and “triggerless” DAQ system in a real measurement: perform the analysis of the **same observable** in the two cases and **compare results**

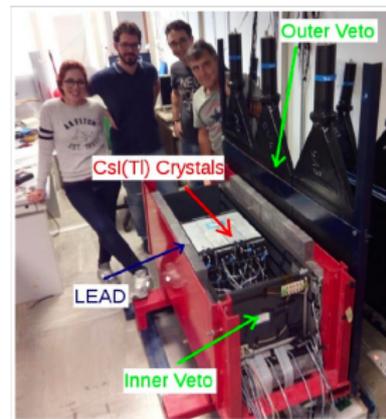
BDX-proto measurement @ JLab:

- Place a small scale prototype of one BDX module in a setup with similar overburden configuration as in the final setup
- Measure cosmogenic rate and evaluate foreseen backgrounds

BDX-proto detector:

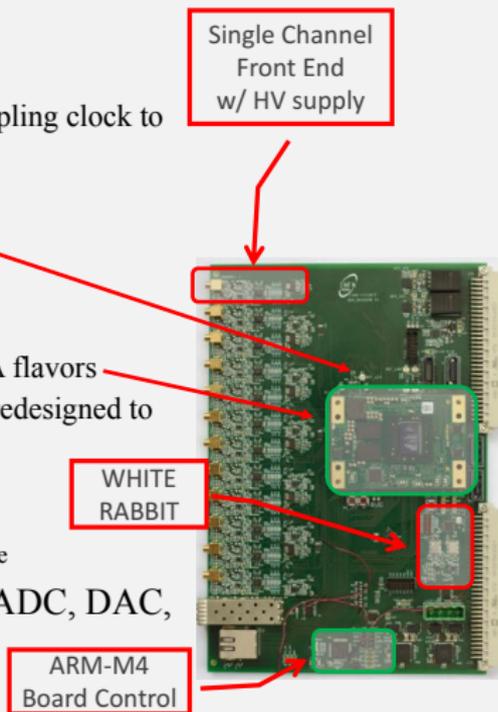
- 16x CsI(Tl) crystals, SiPM readout
- 2 plastic scintillator veto layers, SiPM readout
- Setup to be modified to be compatible (cabling, ...) with wave-brd readout

Tests foreseen in 2019



Board features

- Timing Flexible:
 - PLL to multiply and fan out the sampling clock to FastADCs and FPGA
 - White Rabbit enabled
 - Clock&Time Dedicated inputs
 - Daisy-chainable
- Customizable:
 - COTS SOMs come in various FPGA flavors
 - Maintaining pinout, SOM could be redesigned to fit different projects
 - FastADC is BOM-selectable
 - 12/14 bit resolution
 - 65/125/160/250 MHz max sampling rate
- ARM-M4 for peripheral control (ADC, DAC, PLL, T sensor, etc)



Board features: price range

- Board cost is adjustable to target project
 - Use the right ADC: price ranges from 9 to 65 €/channel
 - Use the right SOM: 500€ to 780€
 - Redesign SOM with simpler/cheaper FPGA

Total cost ranges from 1.3k€ to 1.9k€ per board

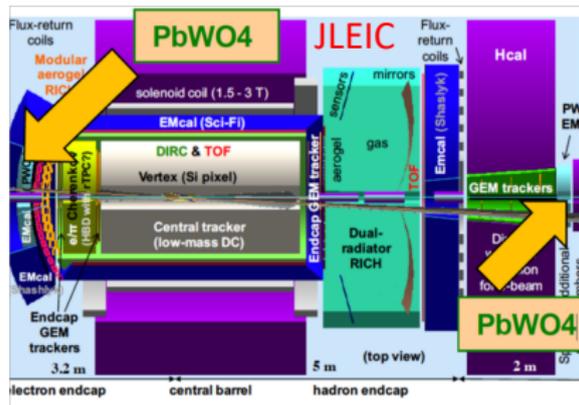
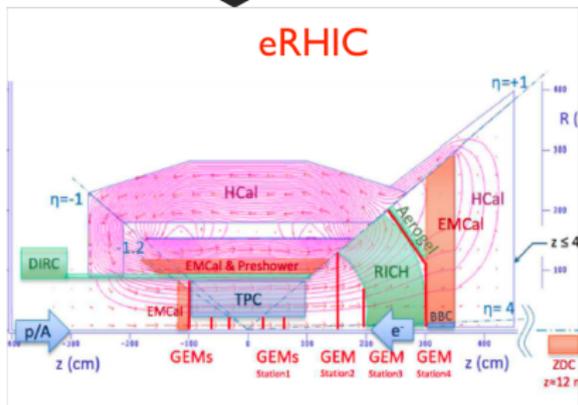


BDX (A. Celentano, F. Ameli)

BDX tests as a first step toward EIC triggerless system validation

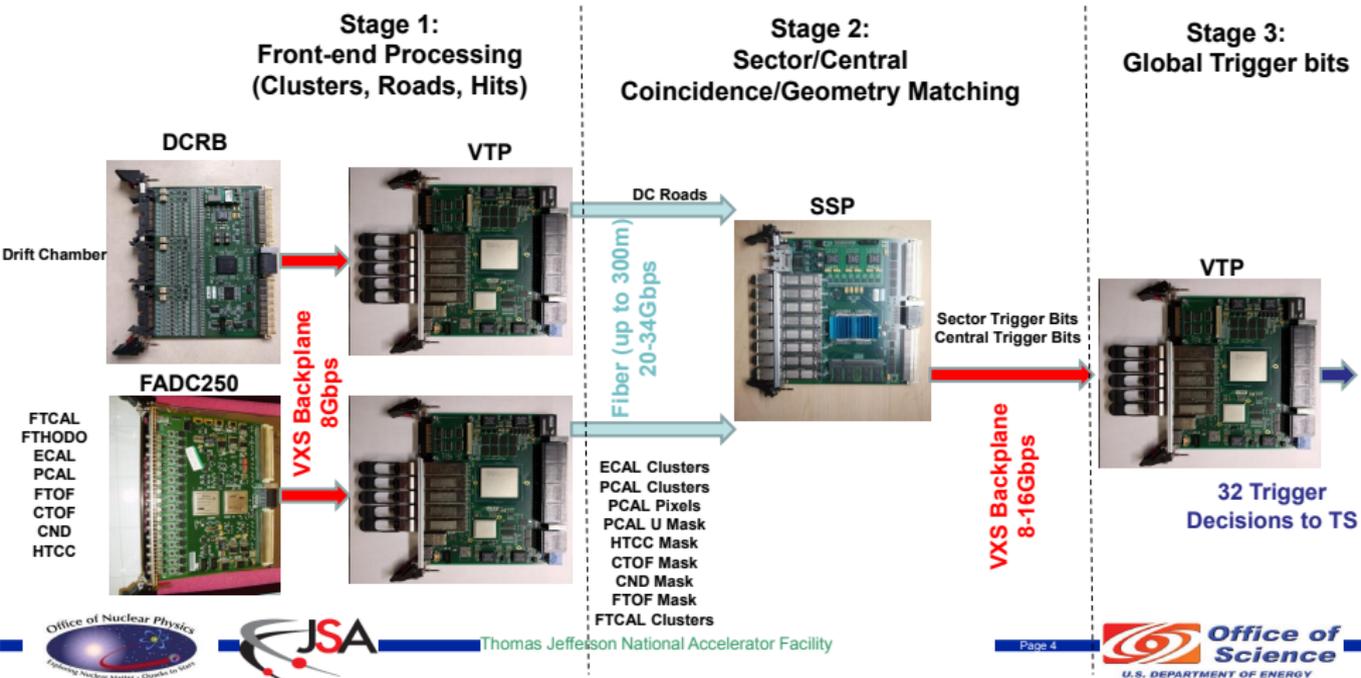
Tests and characterization measurements of a streaming readout system for the BDX setup can be a first step toward the validation of this technology for the full EIC detector – *starting from EM calorimetry*

- **Same technology:** PbWO₄ crystals + SiPM readout
- Number of channels for BDX-Mini large enough to study EM showers measurement and reconstruction
- Software system (TRIDAS) adaptable to other detectors
- Readout board design can be extended to other front-ends
- Rate stress-test is possible by lowering local thresholds at few phe level



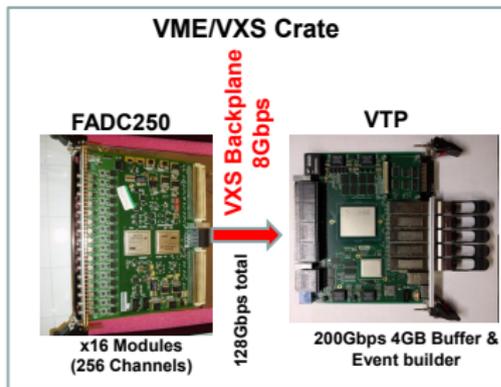
JLAB: Innovation in Nuclear Data Readout and Analysis (B. Raydo, E. Jastrzemski, W. Gu)

JLAB Example Trigger System (CLAS12)

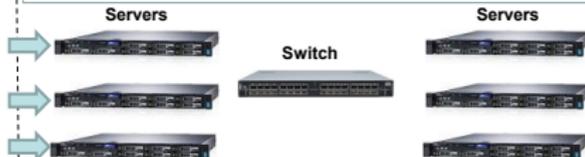


JLAB: Innovation in Nuclear Data Readout and Analysis (B. Raydo, E. Jastrzemski, W. Gu)

Test Setup

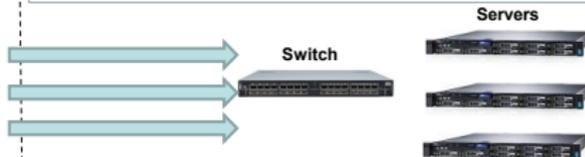


Would prefer this for long-term which would allow simplified & customizable front-ends. Single server serves specific detector channels and is responsible for interleaving events to next layer.



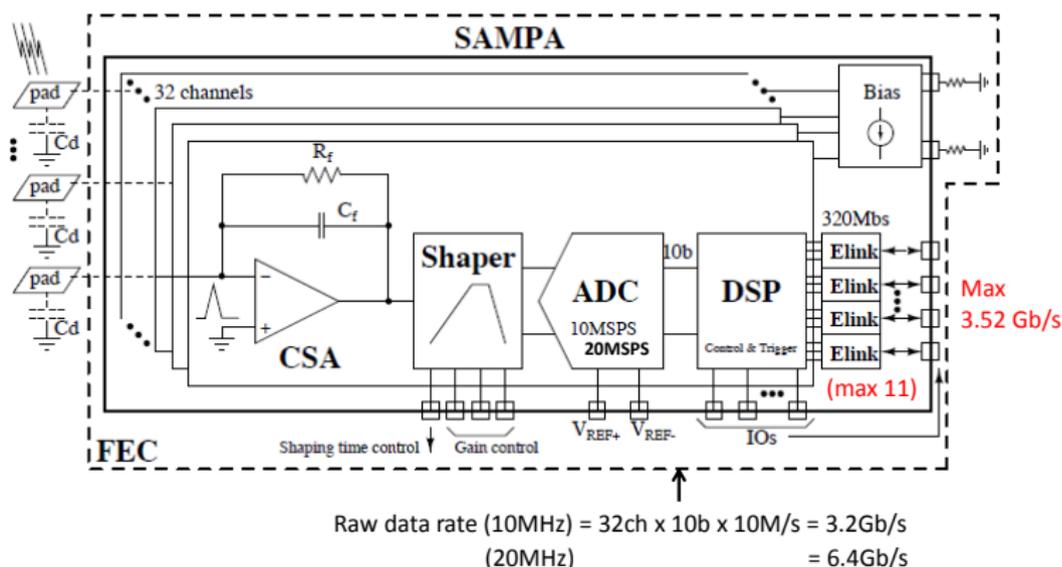
or

Could do this given VTP buffering and TCP capability – VTP interleaves events across servers, but unlikely/unwanted front-end hardware complexity for future developments.



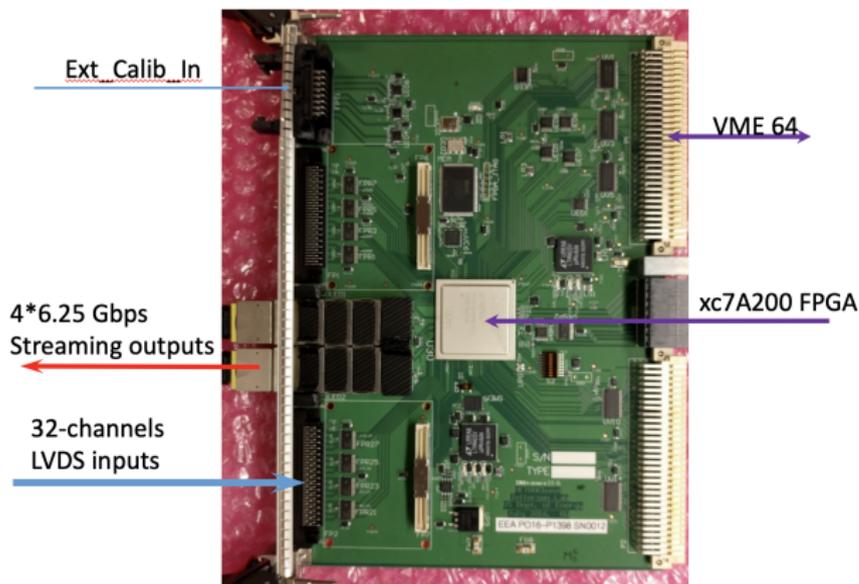
JLAB: Innovation in Nuclear Data Readout and Analysis (B. Raydo, E. Jastrzemski, W. Gu)

SAMPA Block Diagram



JLAB: Innovation in Nuclear Data Readout and Analysis (B. Raydo, E. Jastrzemski, W. Gu)

3.1 Streaming Readout TDC design with VETROC board



Summary



- Alphacore presented the current status of detector readout IC development including rad-hard preamplifiers, ADCs and combined ROICs.
- Large tapeout was completed and IC testing will start in January 2019.

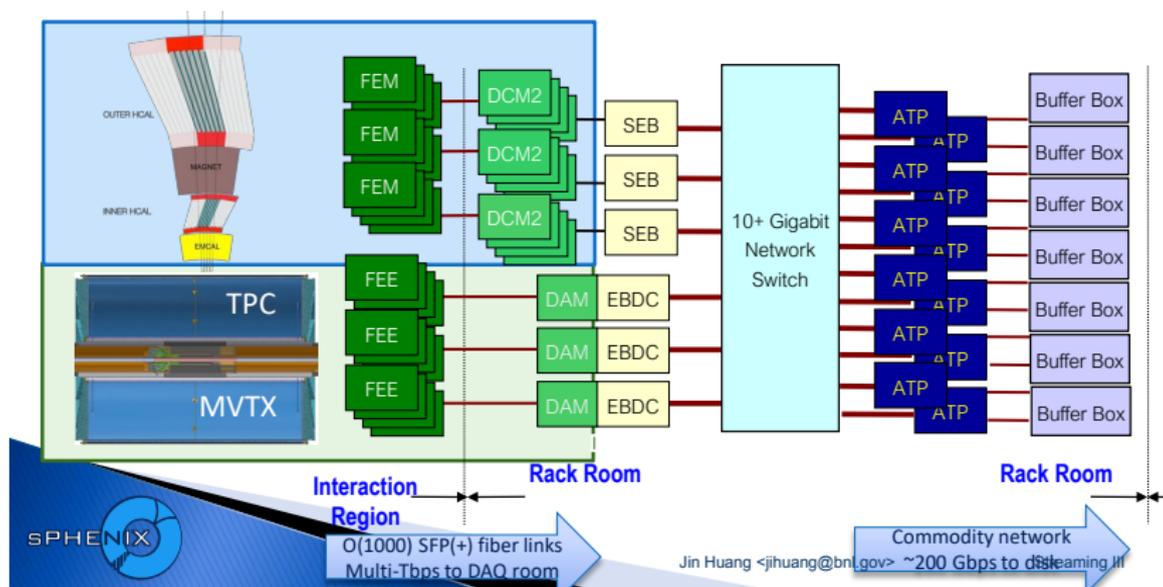
Questions for the audience?

- **Is there a need for a “Combined ROIC”, i.e. a chip that has both preamplifiers and ADCs, or can they be on separate chips?**
- **What are the target experiments, their schedule, channel counts, and readout specifications?**
- **Radiation hardness requirements?**
- **Integration level requirements (IP? Wafers? Packaged chips? Packaged and tested chips? Evaluation boards? Ready-made readout boards with FPGAs ?)**



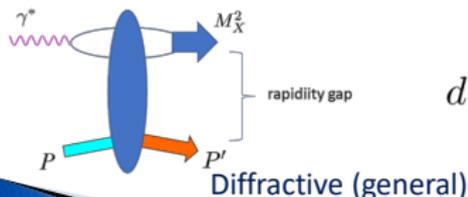
SPHENIX and EIC-SPHENIX (J. Huang)

- ▶ **For calorimeter triggered FEE,**
(signal collision rate $15\text{kHz} \times \text{signal span } 200\text{ns}$) $\ll 1$:
No need for streaming readout which significantly reduce front-end transmission rate
- ▶ **For TPC and MVTX tracker FEE supports full streaming:**
(signal collision rate $15\text{kHz} \times \text{integration time } 10\text{-}20\mu\text{s}$) ~ 1 :
Streaming readout fits this scenario. Consider late stage data reduction by trigger-basec

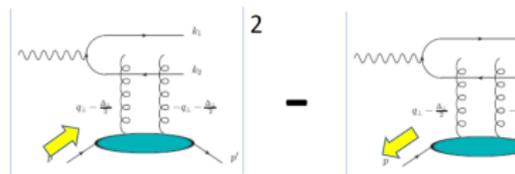


SPHENIX and EIC-SPHENIX (J. Huang)

- ▶ Full streaming readout → DAQ interface to commodity computing via PCIe-based FPGA cards (e BNL-712/FELIX series) → Disk streaming raw data → Event tagging in offline production
- ▶ Why streaming readout?
 - Versatility of EIC event topology make it challenging to design a trigger on all interested event. e.g. new diffractive-type events below, and new type of events not yet envisioned?
 - Many EIC measurement, e.g. SF, are systematic driven. Streaming minimizing systematics by avoiding hardware trigger decision + keep background and history
 - At 500kHz collision rate, many detector would require streaming, e.g. TPC, MAPS
- ▶ Why BNL-712/FELIX series DAQ interface? [More on next slides]
 - 0.5 Tbps x bi-direction IO to FEE ↔ large FPGA ↔ 100 Gbps to commodity computing
 - O(\$100) / 10Gbps bidirectional link
- ▶ Why keep raw data?
 - At 100 Gbps < sPHENIX rate, we can disk all raw data: If you can, always keep raw data.
 - Achieve final minimal systematics may require refining calibration with integrated and special (e.g. z.f.) data
 - Calibration in real-time for final production in real-time requires considerable manpower for preparation (FTE?) and risky to fit in initial running years.



$$d\Delta\sigma \sim$$



Diffractive di-“jet” :

Promising new channel to access OAM

Jin Huang <jihuang@bnl.gov>

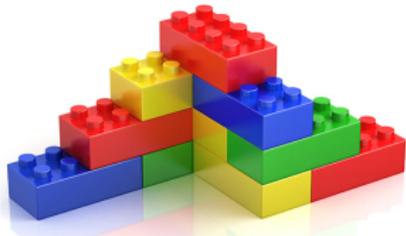
Streaming III



Network and Software aspects (M. Diefenthaler, J.C. Bernauer, D. Blyth)

Streaming readout software requirements

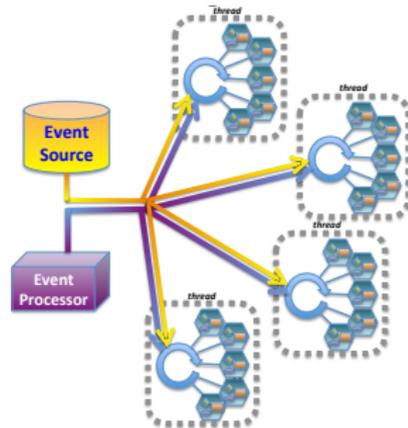
Modular design



Common data model (conceptual logical and physical), instead of common framework



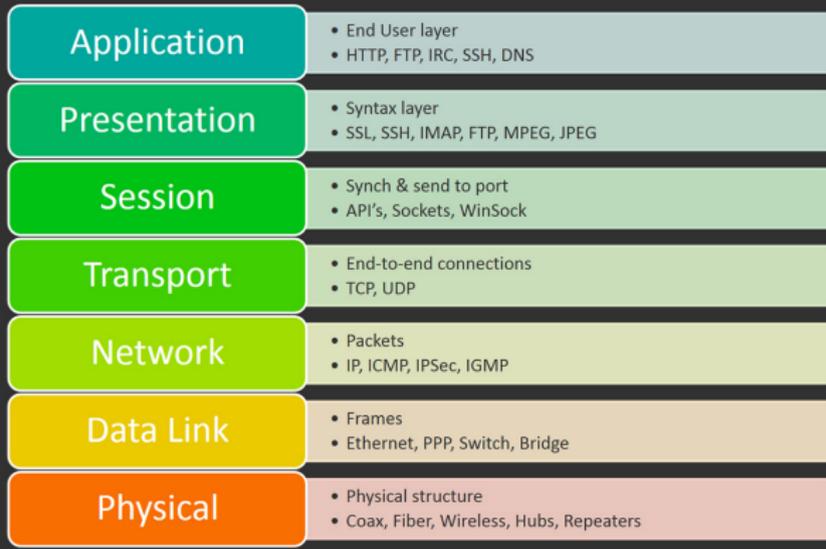
Common parallelizer



Network and Software aspects (M. Diefenthaler, J.C. Bernauer, D. Blyth)

Open Systems Interconnection layers

7 Layers of the OSI Model



Network and Software aspects (M. Diefenthaler, J.C. Bernauer, D. Blyth)

Wish list for Presentation Layer

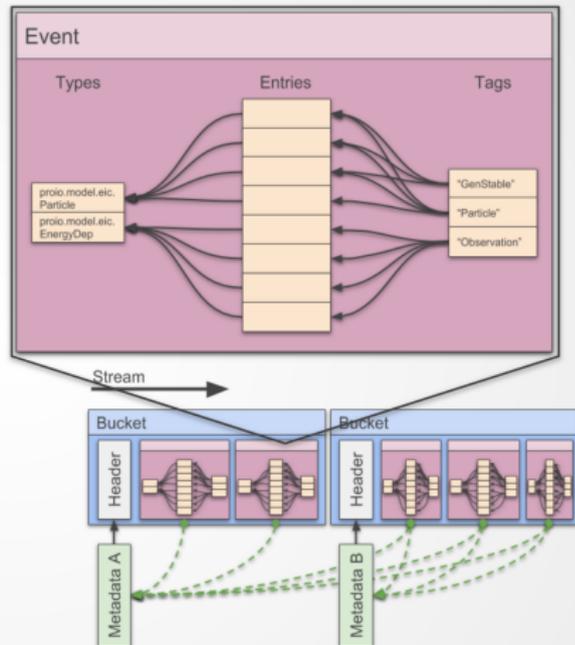
- Efficient implementation on CPU and FPGA
- Easy to add/drop substreams, parts of streams.
- Must decode enough without configuration
- Empty channels need 0 bytes
- Flexible for wide range of data types
- Self-documenting
- Bindings to many languages

Network and Software aspects (M. Diefenthaler, J.C. Bernauer, D. Blyth)

ProIO

- project for utilizing protobuf for HEP/NP in a language-neutral way
 - C++, Python, Go, and Java native libraries already implemented*
- supported by ANL LDRD and eRD20 (multi-lab EIC Software Consortium)
- based on pioneering work by Sergei Chekanov (ProMC) and Alexander Kiselev (EicMC)
- <https://github.com/proio-org>
- preprint available end of this week (contact me at dblyth@anl.gov for copy)

*Java implementation is currently incomplete, but read functionality is there



- Streaming readout is a reality, many experiments going this way.
- Many SRC members work on different aspects, but we need to coordinate to come to focused EIC effort. Need resources to do so.
- Need to work together with other consortia, readout, detector and physics development are intertwined!

- Compare approaches of the different existing streaming readout systems for technical questions
 - Timing distribution
 - Network architecture
 - ...
- Prototype on-wire protocol specification
 - Request For Comments style
- Try to answer how benefits seen by other projects translate to EIC
 - Reach out to EICUG

Next workshop

- Next workshop will be in **Camogli, Genova - Italy in May**
- Two full days
- EIC progress, but also reports from other projects
- Hope for many contributions from EU labs
- Progress on ongoing projects
 - Hardware
 - Working prototype streaming readout
 - Validation of streaming vs. triggered readout

We will use the awarded funds to offset the workshop costs / invite speakers.