Project Description:

Submitting Institution: Thomas Jefferson National Accelerator Facility
Experimental Nuclear Physics Division
Fast Electronics Group

Project Title: Front End Readout Module for Detector Data Acquisition and Trigger System

Project Abstract and Relevance to EIC

The proposed EIC design emphasizes high luminosity (~10^{34}) to access small cross section probabilities and allow for multi-dimensional mapping. For the envisioned luminosities, expected e-p rates are high requiring a sophisticated data acquisition trigger system, with multiplicities even higher for e-A interactions.

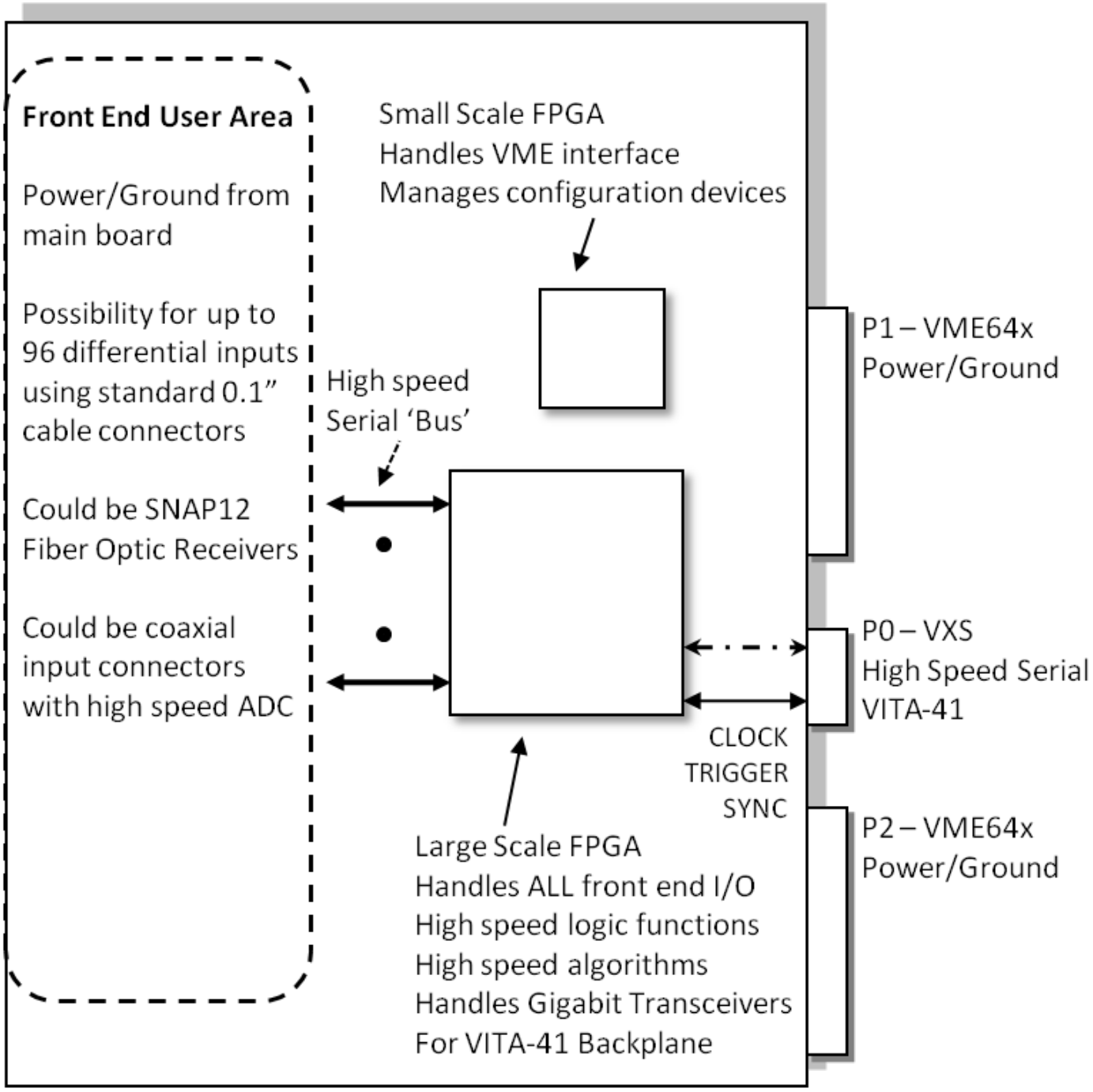
Readout hardware will be needed in the immediate future to support collaboration groups that are designing apparatus for the various detector regions of an EIC or e-A experimental program. The need for flexible front end readout electronics that allows detector R&D groups to test high input rate conditions and develop custom algorithms to reduce data readout size per event trigger is the motivation for this proposal. The flexible front end format will be defined so that many different circuit configurations can be applied to interface directly with the specific circuitry that resides on the detector apparatus. The front end flexibility would cover a wide range of connector and signal types, from standard coaxial cable from Photomultipliers, to multichannel ribbon cable typically used for wire chamber preamplifier outputs. A larger circuit board area will allow for higher channel density on the front panel, and the control, high speed data bus, plus high speed serial interface are included by using the VITA 41 standard backplane.

Design Approach

We will use our successful experience with the VITA 41 high speed serial backplane as the DAq and trigger system interface. The custom Front End Readout Module (FERM) would be designed on a 9U x 220mm board format and would use our existing VME64x interface, supporting 2eSST readout speed, and also interface with the VITA 41 Gigabit backplane connections. Presently only two Gigabit serial lanes are used at transceiver speeds of 2.5Gb/s per module, but we propose to use all four serial lanes at 5Gb/s so that the aggregate data speed for passing trigger information per module would be 16Gb/s. With this type of bandwidth per module, real time trigger algorithms could be performed on detector input signals. Consider that energy summing is accomplished for sixteen 12bit ADC with existing FPGA hardware, and the proposed design would add enough bandwidth to perform calorimeter cluster finding algorithms in addition to simple digital summing functions.

The FERM would be designed with two main sections. The bus interface section which manages the VME64x and VITA 41 high speed serial Gigabit signaling, and the input signaling section which would be designed on a modular (mezzanine) platform to handle different style connectors coming from various detector types. For instance, traditional photomultipliers use coaxial cable, and drift chamber signal cables are typically differential analog, or differential logic level. The input signaling section would be designed to interface with the specific detector cabling, and the FERM's bus interface section would remain constant. A block diagram is shown in Figure 1.

Figure 1: Front End Readout Module: Block diagram



9U x 220mm single width VXS "Payload" format

R&D Experience

The 12GeV experimental program at Thomas Jefferson National Accelerator Facility will rely on custom pipelined front end DAq and trigger modules that are fully synchronized at 250MHz. These modules are designed to utilize the VITA 41 high speed serial backplane for data acquisition and transmission of trigger information from each front end crate. Production designs are nearly complete for several of these custom modules and will be ready for installation to meet the 12GeV schedule.

Presently, the front end modules are designed using commercial ADC that sample detector signals at 4ns intervals with 12-bit resolution. Commercial ADC modules are available with faster sampling rates, but we propose to develop a Front End Readout Module that has a higher channel density, and provide feature extraction algorithms that will be included in the overall global detector trigger decision. Higher channel density using a larger 9U board size would reduce overall module and crate count and this format could be applied to interface with the different detector readout devices and cabling.

The proposed FERM design would offer significant circuit board design challenges such as power and cooling, plus high speed layout and signal integrity issues would need additional modeling and simulation. We have the required Computer Aided Engineering and Computer Aided Drawing (CAE/CAD) software for creating new component schematic libraries, board schematic diagrams, and complex multilayer circuit boards. We have also invested in simulation tools from Mentor Graphics that verify signal integrity of controlled impedance high speed multilayer circuit boards.

We have completed R&D with the VITA-41 high speed serial backplane, and gained valuable experience with production versions of several complex custom modules that use multiple large scale Field Programmable Gate Arrays(FPGA). The FPGA are from well known industry leaders, Xilinx and Altera respectively, and we have several experienced firmware (VHDL) design engineers, that have successfully implemented these FPGA and the Gigabit transceivers that are embedded on these devices. Present FPGA technology allows 5Gb/s per serial connection, and we bond multiple serial transceivers to achieve the bandwidths required to produce trigger signals at a 200KHz rate, with less than 4us overall latency.

System level distribution of the 250MHz global sampling clock, synchronization signal, and trigger signals are handled with commercial Gigabit (3.125Gb/s) fiber optic transceivers from Avago. We have successfully demonstrated a zero latency trigger distribution with fiber optic cabling where the difference in fiber optic cable lengths is over 100m between readout crates.

At Jefferson Lab the Data Acquisition system is not driven by a beam crossing clock, and scores of successful experiments have been completed with the 499MHz beam 'bunch' on fixed targets... A trigger occurs when the trigger condition is satisfied, which is computed asynchronously to the beam crossing rate.[1] For the proposed EIC the interaction rate = $\mathbf{x\sigma}$ will be approximately ~100kHz, where an e-p interaction of interest occurs every beam crossings, even at an RF beam structure of 1.5GHz

R&D Expected Results

The primary focus of this R&D proposal is the extend our engineering experience and increase the input channel density and versatility of the input section for a front end detector readout module that will benefit the detectors proposed for the interaction areas of the EIC. Coupled with this front end focus is the expectation to increase the bandwidth of the Level 1 trigger information streams that will exceed our most recent design specifications. The proposed design format would allow many different types of input signals from the various detector types proposed for the EIC interaction areas. As an example, the higher channel density detectors near the interaction area (lowQ^2), will be readout with custom Application Specific Integrated Circuits(ASIC)

similar to silicon trackers at Fermi Lab.[2]. The FERM would provide a flexible hardware framework so that the output of the ASICs would properly synchronized to the pipeline DAq system, and ASIC readout data would be processed and significantly reduced by algorithm on the FERM data processing FPGA.

A comparison in Table 1 lists performance specifications for an existing VXS front end board design, and the proposed specifications for the Front End Readout Module.

Parameter	**Existing Design**	**FERM proposal**
#of channels (Coax)	16	24
# of Bits/channel	12	10-12
Sample rate	250MHz	250MHz – 500MHz
Fiber Optic transceivers Data input capability	8 - (MTP- 4Tx/4Rx) 80Gb/s	12 Rx- (SNAP12 or Avago Modpac) 360Gb/s
VME2eSST	Yes	Yes
VXS transmission rate Aggregate (8/10b encoded)	2 Rx/Tx at 2.5Gb/s 4Gb/s	4 Rx/Tx at 5Gb/s 16Gb/s
#Channel/Crate(Lemo Coax)	256	384
Flexible input design	No	Yes

Table 1: Specification comparison

Deliverables

All CAE/CAD files required to design, simulate, including VHDL source code and final firmware will be the primary deliverables for the initial year of R&D for this project. Assembly and fabrication data needed to order a prototype module in industry, plus a complete bill of materials spreadsheet that lists details of the required integrated circuits, connectors and mechanical hardware such as front panel and heat-sinks will also be part of the project documentation, and will be considered the hardware fabrication phase of the project in year two. The hardware fabrication phase of the project will require significant testing activities and include a requirement for additional test and measurement equipment to verify Gigabit serial performance of the proposed FPGA transceivers.

Required Resources and Equipment

Existing infrastructure exists at Jefferson Lab, and we have managed to build up a new CAE/CAD library of the components and integrated circuits that are used for the complex multilayer circuit boards that typically consist of several large scale FPGA. The activities required to meet the deliverable goals listed in the previous section will require at least 22 weeks (0.5 FTE) of an electronics design engineer coupled with at least the same number of weeks for an electronics designer/technician to support schematic capture, board layout and test of required sub-circuits and component research.

Year two of the project, would initiate the purchase of the circuit board(s), components, and prepare the required files for the assembly of at least one full prototype module. During this phase of the R&D project, a new Digital Signal Analyzer (DSA) or equal Digital Sampling Oscilloscope (DSO) would be required to accurately measure and verify the higher digital serial transmissions that have been proposed. Currently our Tektronix DSA70000 has the bandwidth (8GHz) to cover at least the first 5 harmonics of our 2.5Gb/s links. The 5th harmonic is strongly recommended for Gigabit backplane measurements by oscilloscope vendors and signal integrity experts. To meet and exceed the performance goals of the proposed R&D project, using 5Gb/s FPGA transceivers and higher speed fiber optic devices, we will need an upgrade to our existing test equipment.

Funding request(per year)

Table 2 shows an outline of the activities for each year of the FERM project. Cost is shown as burdened (overhead included) and is consistent with past delivery experience for complex board projects required for the 12GeV experimental program. The activities and equipment listed for the 2nd year could be funded over the course of an additional 3rd year if necessary.

Year	Activity	Deliverable Description	FTE	Cost($K)
1	*Design*	Full Specification and component research Schematic capture CAD files Component placement - CAD file Circuit analysis and layout - CAD files HyperLynx simulations(Board stack) Board routing - CAD files Verification - Power analysis data Firmware specification report Firmware development - VHDL files Firmware simulation(functional) Firmware test(post place/route) Documentation report	0.5 EE 0.5 ED	$120K
2	*Full Prototype Fabrication/Assembly*	Full verification of fabrication/assembly Files for industry order - BOM Procurement - Components Procurement - Front panel/Mechanical Procurement - Board/Assembly		$15K
2	*Full functional Test* *Test equipment* *Test/Documentation*	 Upgrade or new Digital Serial Analyzer ---------- Assembly inspection report Power verification report Firmware - Functional test report Firmware - Full verification test report Performance test measurements Performance analysis report Operational Guide - Documentation Engineering Change Orders list	n/a 0.5 EE 0.5 ET	 $75K $120K

Table 2: Activity/Deliverables and Funding request

[1] "DAQ & Trigger Electronics for the CW Beam at Jefferson Lab", Ben Raydo, EIC Collaboration @ Stony Brook January 10-12, 2010

[2] "Fermilab Silicon Strip Readout Chip for BTeV",IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 52, NO. 3, JUNE 2005