

Forward Calorimeter Readout Electronics

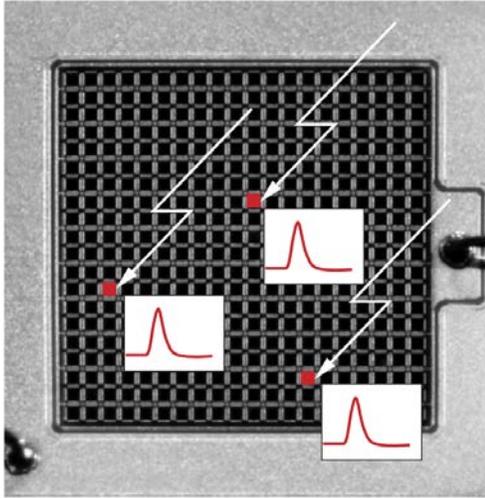
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RHIC Spin collaboration meeting 3/9/2017

Silicon photomultipliers

[Figure 2-2] Image of MPPC's photon counting *



A Geiger-mode APD is an APD operated such that the avalanche grows without bound until limited externally. It produces one pulse of fixed amplitude when triggered, with no proportionality to the initiating event.

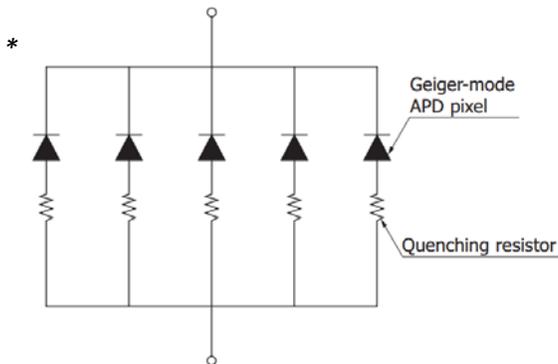
A silicon photomultiplier, aka MPPC, is simply an array of Geiger-mode APD's with a quench resistor for each, connected in parallel. Initially biased at a voltage above the avalanche breakdown voltage of the APD cell, the diode voltage drops just to the breakdown voltage when it is triggered and then the avalanche quenches.

Signal size (output charge per pixel fired) is simply

$$C \cdot (V - V_{BR})$$

Under low level illumination, the SiPM produces a pulse proportional to the number photons, like a PMT.

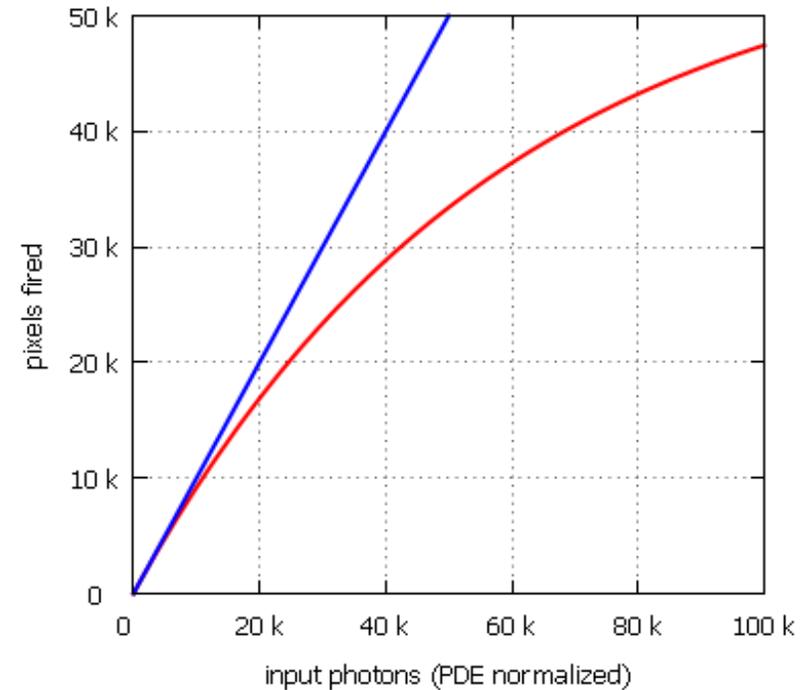
Time structure of the pulse *if not limited by the external circuit* is basically a fast step and exponential decay with RC time constant determined by the pixel capacitance C and quench resistor R. Sub-nanosecond risetimes are typical.



Hamamatsu S13360 25 μm pitch SiPM parameters: $C = 22 \text{ fF}$, $R = 690 \text{ k}\Omega$ ($RC = 15 \text{ ns}$), $V - V_{BR} = 5 \text{ V}$

Basic properties

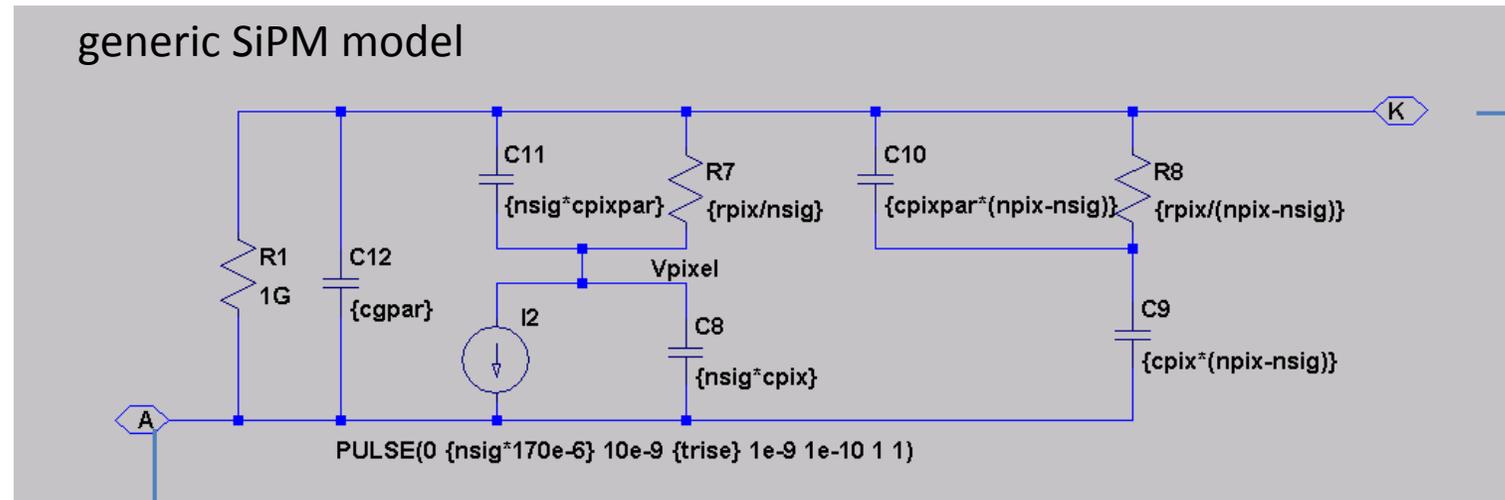
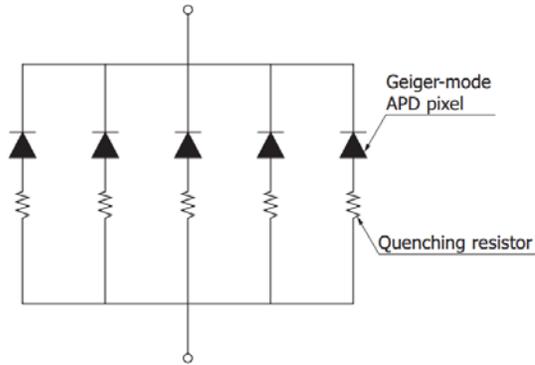
- Immune to magnetic fields, unlike PMT's 😊
- Compact / low mass
- Not immune to radiation, unlike PMT's 😞
- Quite high dark count rate: $\sim 5 \text{ MHz/cm}^2$ before, to over 1 GHz/cm^2 after irradiation (to 10^{10} n/cm^2)
- Relatively low voltage operation (20 – 70 V depending on type)
- High stability bias required: 1% gain error \leftrightarrow 50 mV \leftrightarrow 800 ppm bias voltage error
- Strong temperature dependence of VBR: $+54 \text{ mV/}^\circ\text{C} \leftrightarrow -1\%/^\circ\text{C}$ gain tempco
 - Easily addressed by bias voltage temperature compensation circuit
- Per pixel there is saturation and deadtime upon detecting a photon
 - Finite number of pixels \rightarrow nonlinearity in response
 - For linear response to high light level, need small pixel size and relatively larger area
- PDE can be better than PMT, but limited by dead area for small pixel sizes: 50% for large pixel, 25% for $25 \mu\text{m}$ pixel



Inherent nonlinearity of simultaneous pixel firing in 57,600 pixel SiPM.

In general $F = N \cdot (1 - \exp(-A/N))$.

Shunt impedance issues



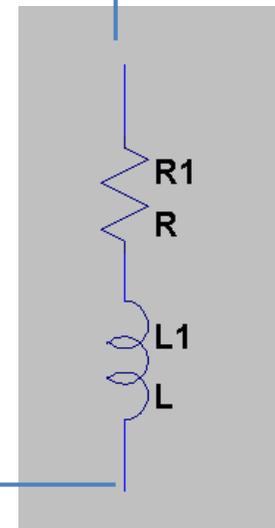
For good signal/noise ratio, most of the charge has to get into preamp on the required measurement time scale. Preamp impedance and bypass capacitor impedance must be low compared to spectator pixels!

fired pixels
(few, proportional to light signal)

spectator pixels
(many, proportional to active area)

Large area SiPM is a very low impedance detector ☹️

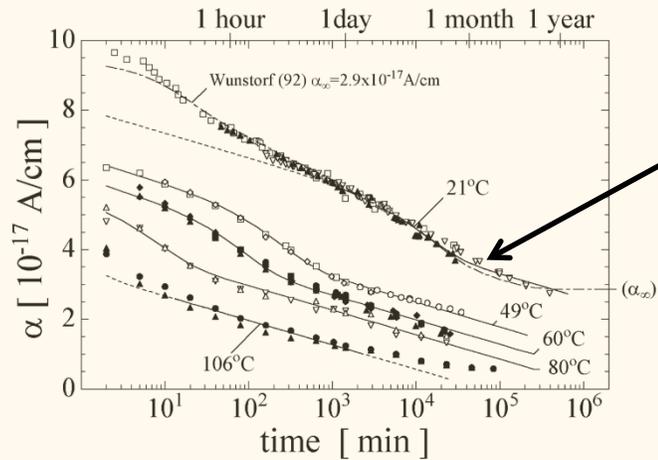
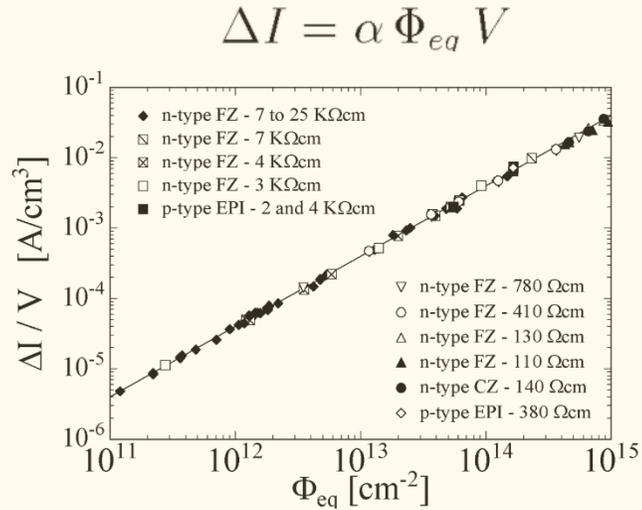
Equally important, for good resolution at high light levels, all of the pixels that fire have to be at the set bias voltage before firing, so they are counted equally.
→ Again external circuit impedances must be very low!



Load impedance model (preamp)

Radiation damage

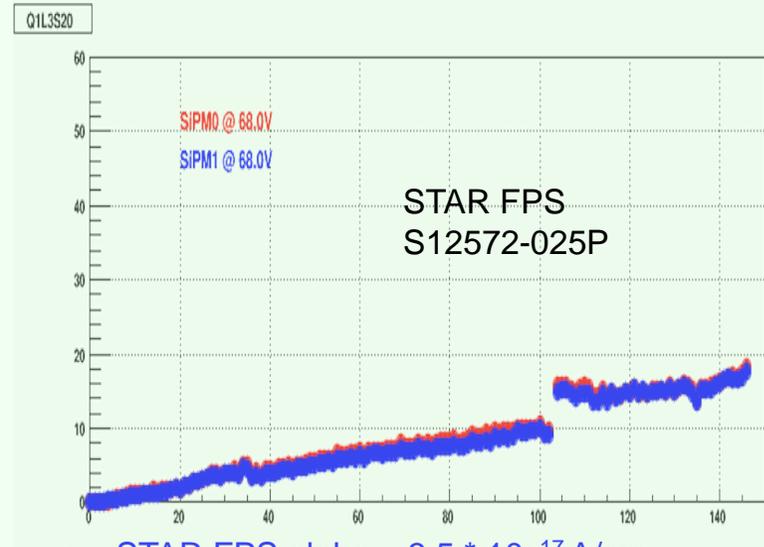
SiPM Leakage Current vs neutron fluence expected vs measured at RHIC Run15 (STAR and PHENIX IR)



M. Moll Phd.Th.

For SiPMs effect is the same as in normal junctions:

- Independent of the substrate type
- Dependent on particle type and energy (NIEL)
- Proportional to fluence



- STAR FPS alpha = $3.5 \times 10^{-17} \text{ A/cm}$
- Thickness of depleted region ~5 μm, Gain 5×10^5
- At 10^{10} n/cm^2 I = 9 μA, Measured 10 μA

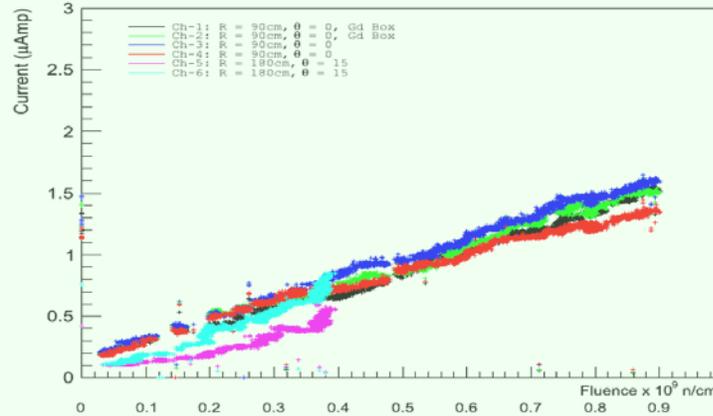


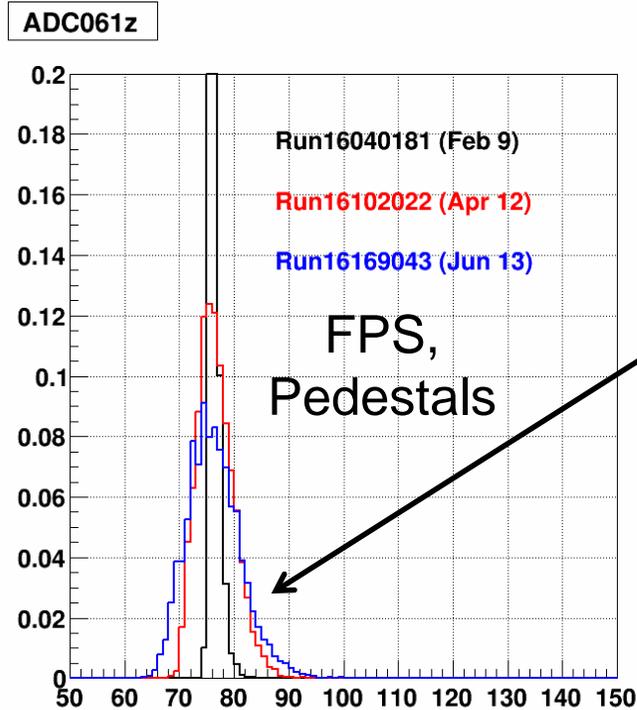
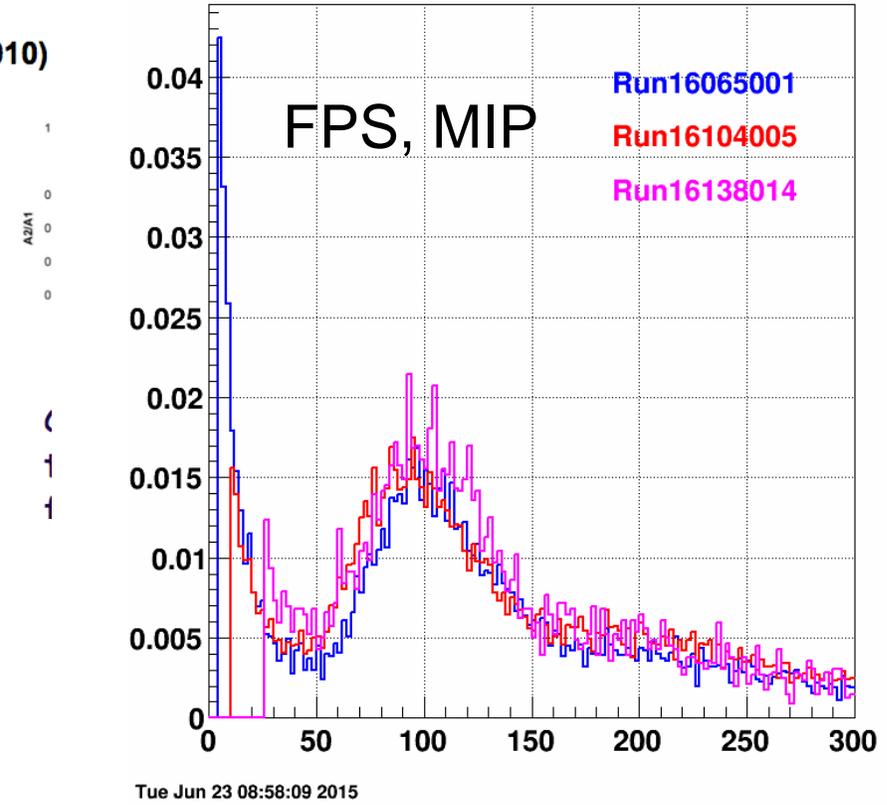
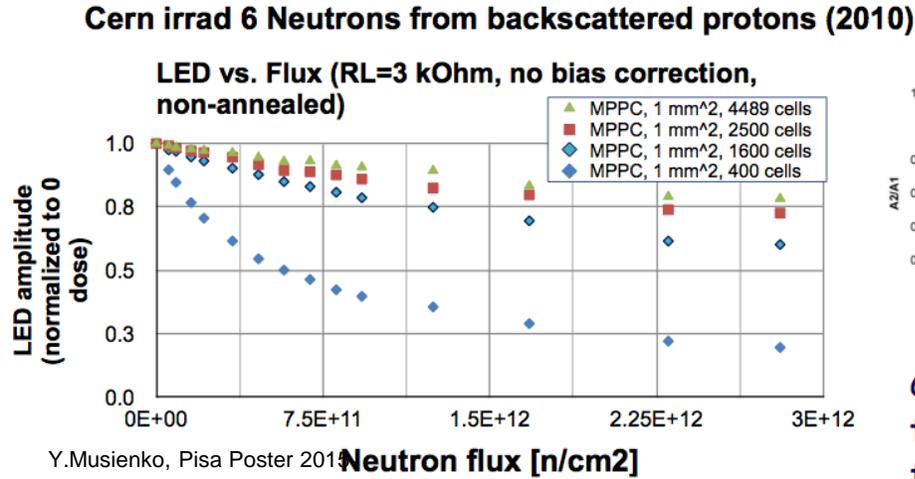
Fig. 8. Hamamatsu S12572-015P SiPMs placed in the PHENIX IR during the current RHIC run. Channels 1&2 were enclosed in a Gd box that absorbed all thermal neutrons. Channels 3&4 were unshielded in the same location. Channels 5&6 were also unshielded and located at the base of the central magnet next to a SPACAL block.

→ S13360-6025
DCR 400 MHz @
 10^{10} n/cm^2

Radiation damage

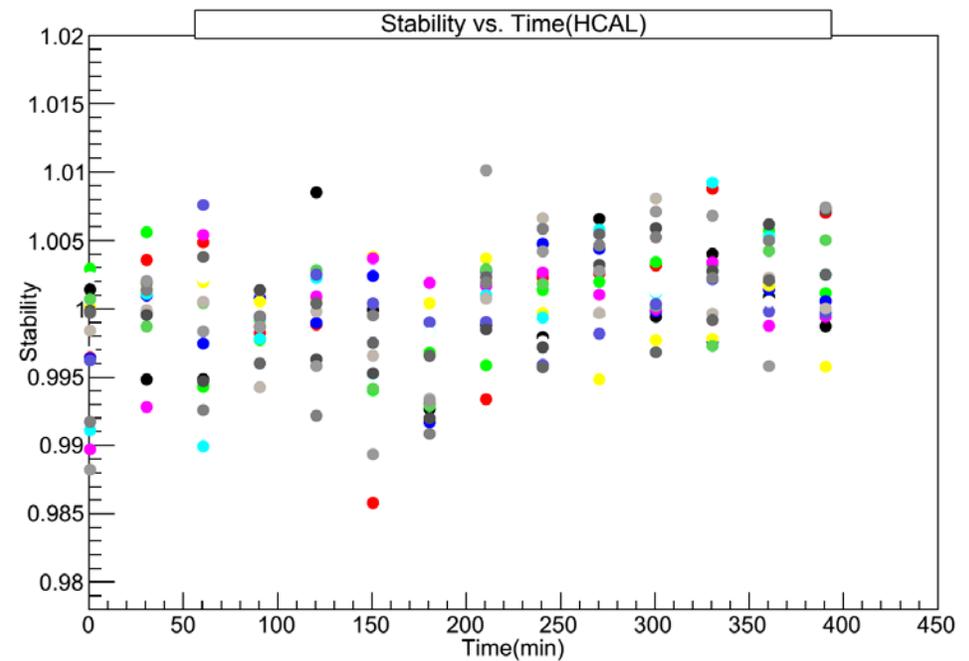
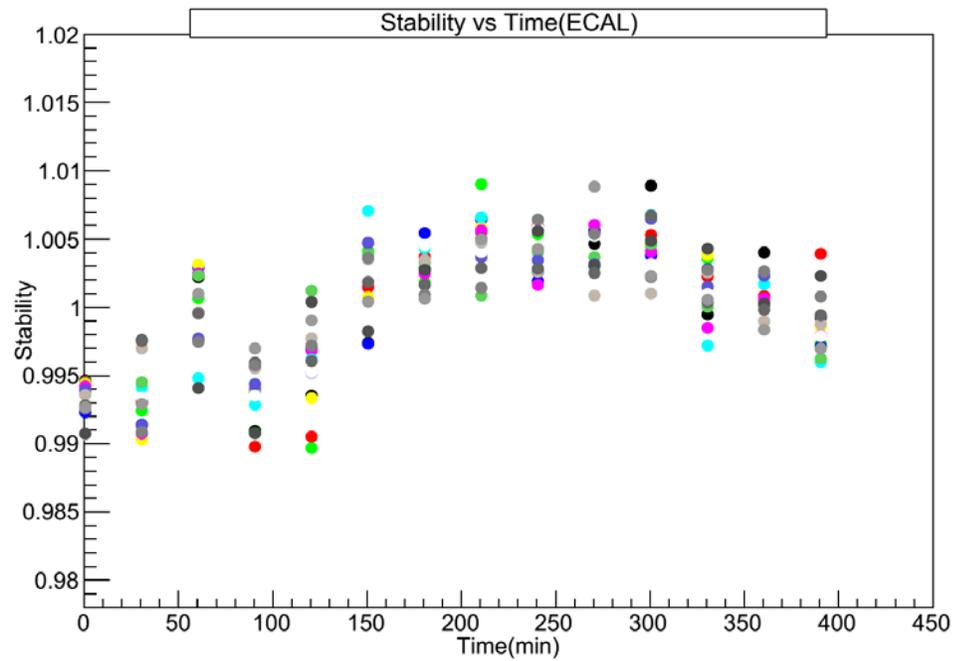
SiPM 'Gain' Stability, Noise :

Q1L1S01



- Two 3x3 mm² Hamamatsu S12572-025P SiPMs per channel.
- Noise ~ 5 p.e. in ~65 ns integration window. Increased 5 times.
- Verified predictable changes in SiPM characteristics under irradiation in **real experimental environment**.
- No significant change (-0.2%) in PDE at 10¹⁰ n/cm²

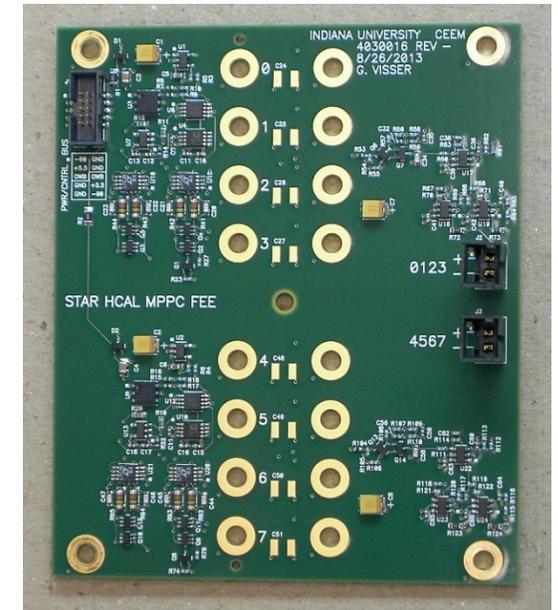
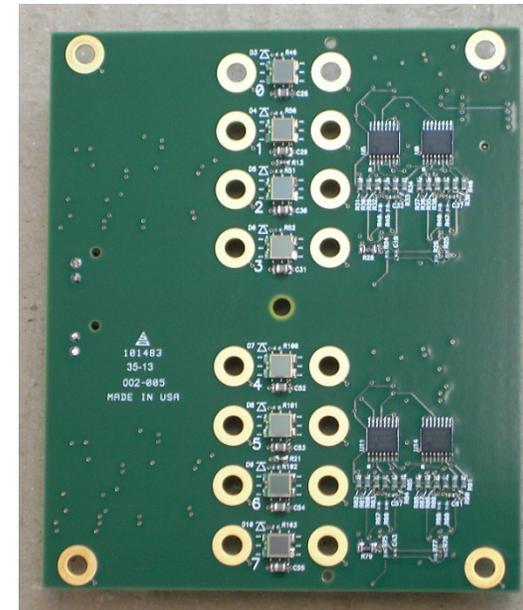
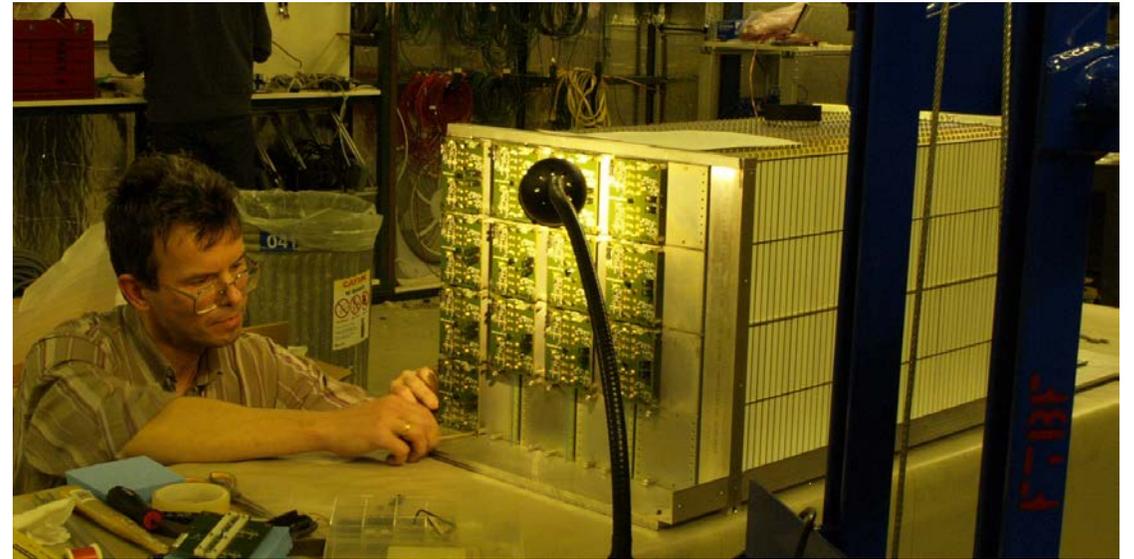
Gain stability during FNAL test run 2014



HCAL readout for EIC R&D (Feb 2014 @ FNAL)

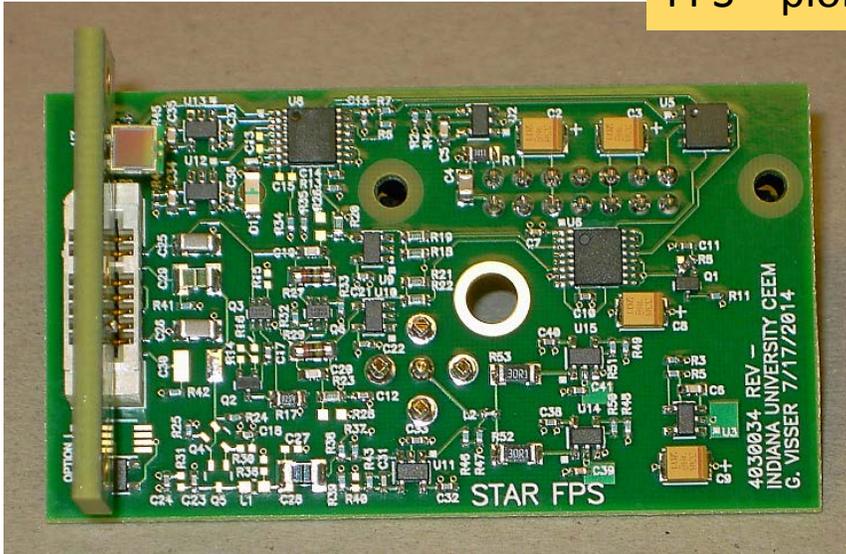
- The first “full featured” SiPM frontend effort from STAR
- Each tower read out by 8 SiPM’s, desired signal is sum
 - Decided (for semi-historical reasons) to use two completely independent groups of four
- Each half FEE has 4 SiPM’s with independent local bias voltage regulation and common bias temperature compensation
- 4 SiPM’s connect in parallel to one preamp / signal path
- differential output, lightweight and low cost cables
- slow controls via I²C on board, and Dallas Semiconductor “1 Wire” bus globally – somewhat slow, but extremely simple hardware and only one wire needed

Breaking new ground in simplicity (of interface) and compactness / low mass for this type of readout



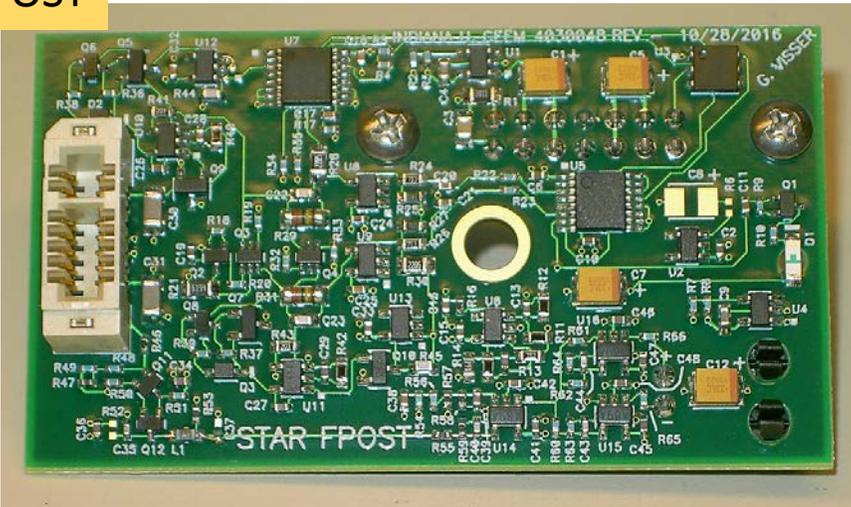
STAR FMS Preshower (2015+) and Postshower (2017+)

FPS – pioneering the use of SiPM’s for physics at RHIC!



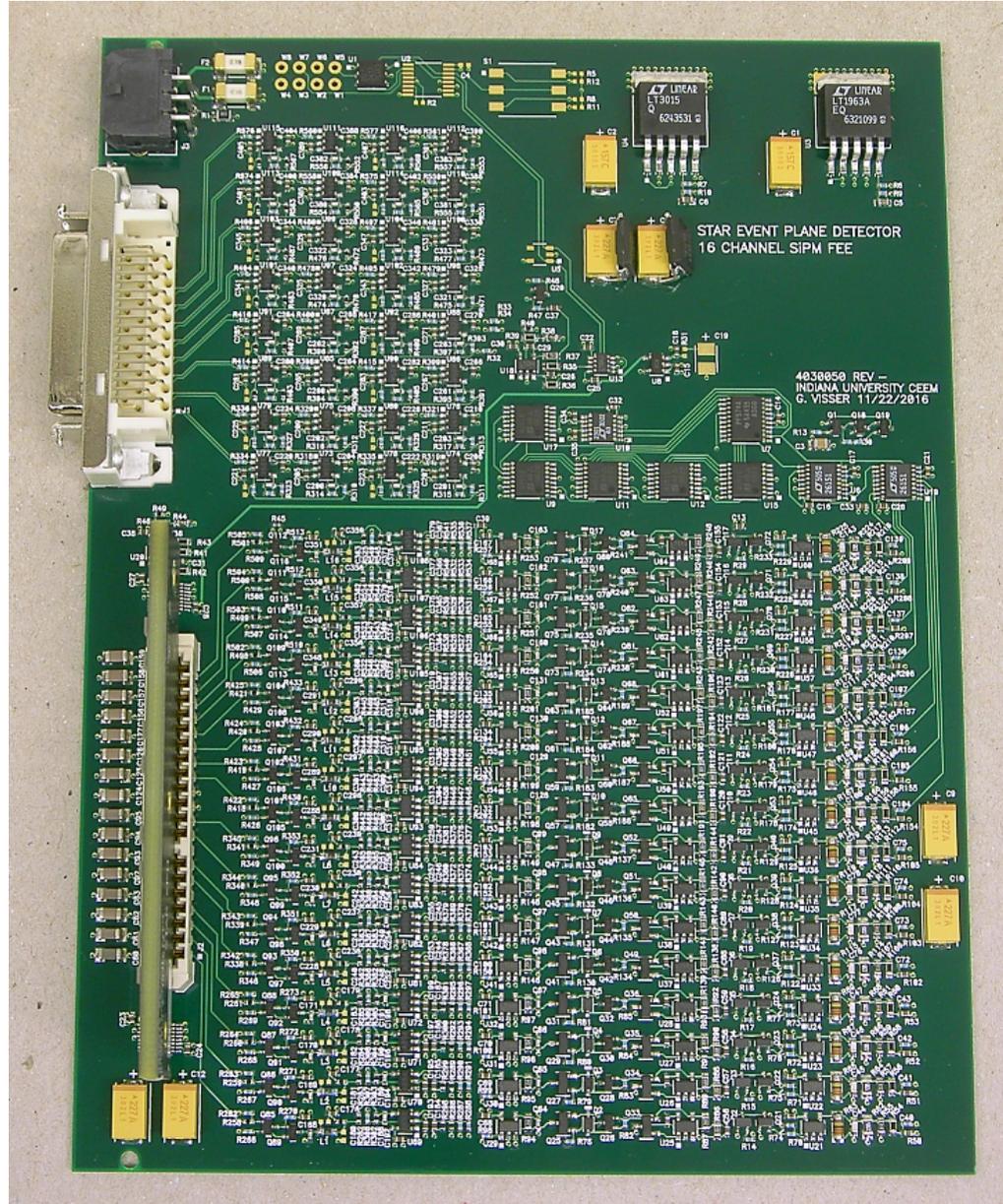
- Based on EIC R&D HCAL FEE, almost the same circuit
- 2 SiPM’s, independent voltage regulation (common temperature compensation)
- Per-SiPM current monitor (0 – 52 μA) – **new feature**, motivated mainly for R&D purposes
 - *For the current monitor, AC coupling of readout was used*
- Single-ended output, designed to drive “QT board” (the workhorse gated integrator ADC used in STAR; 12 bit, 1 nC FS, 70 ns gate)
 - There is some difficulty in doing this with low supply voltage and reasonably low power. Future ADC’s should be more sensitive...

FPOST

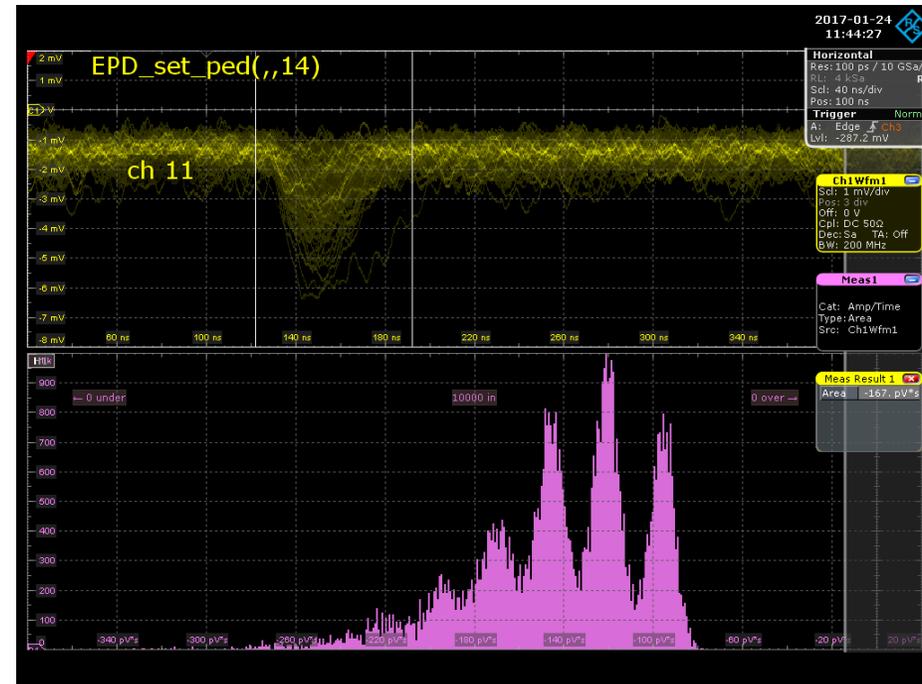


- Based on FPS. No changes to SiPM board, controls, power, mechanical
- Improved noise of bias voltage regulator, $\sigma < 100 \mu\text{V}$
- **DC coupled readout** again – eliminate possible baseline wander, rate dependence
 - This required more complex, “high side” current monitor circuit; works well!
- Current monitor range increased to 151 μA since FPS came close to using up 52 μA range already...
- Output scheme changed back to differential (as in EIC R&D HCAL FEE), new receiver board built to interface to existing QT board
- Lower cost, ~noise-immune signal cables

STAR Event Plane Detector (2017+)



- 16 channel integrated FEE
- 16 SiPM's S13360-1325PE (1.3 mm²) mounted similar to FPS/FPOST SiPM's
- 2 – 3 m fiber cable comes from detector, fiber holder block (LBL) positions over SiPM's
- FEE circuit similar to FPOST except:
 - Lower SiPM current range to 20 μ A
 - Further noise reduction in bias voltage regulator
 - Faster slow controls interface option added – *not tested yet*
 - Cost reduction by change of DAC & ADC parts and amortizing infrastructure over more channels



few-pixel
spectrum,
integration
gate 70 ns

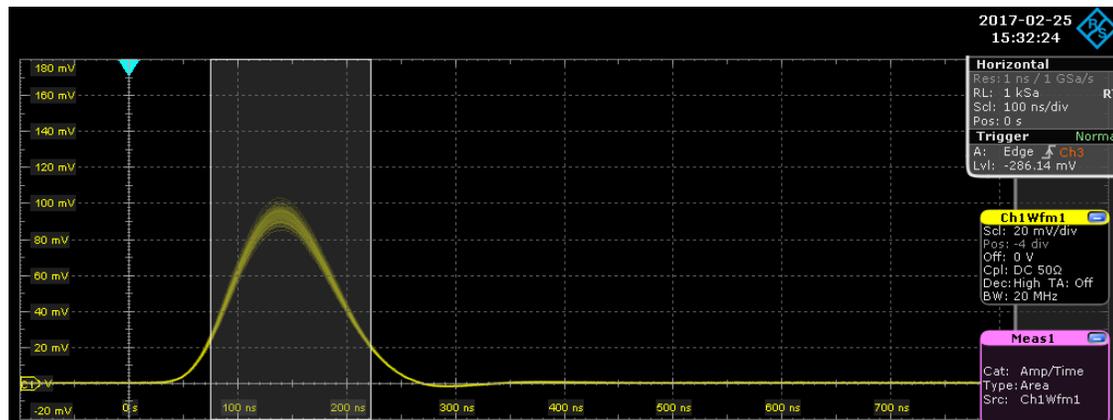
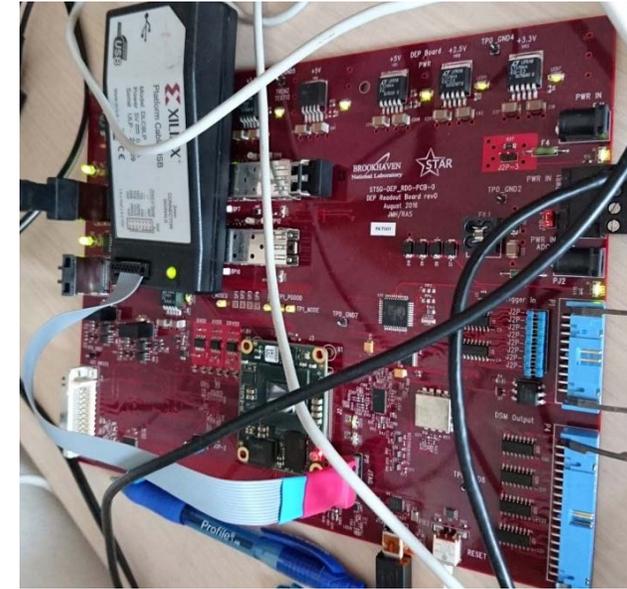
	EMCAL	HCAL
sensor	6x6 mm ² (S13360-6025)	(4 – 6)× 3×3 mm ² (S13360-3025)
N	57,600	57,600 – 86,400
light yield	250 – 500 pixels/GeV	150 pixels/GeV
full scale signal	25k – 50k pixels	15k pixels
dark counts in 180 ns “gate” – initial	0.3	0.3 – 0.4
dark counts in 180 ns “gate” – @ 10 ¹⁰ n/cm ²	72	72 – 108
dark count rms	8.5	8.5 - 10
electronics noise budget (rms)	10	10 – 13

FCS' EMCAL prototype readout

SiPM (on plug!) and pre-prototype frontend

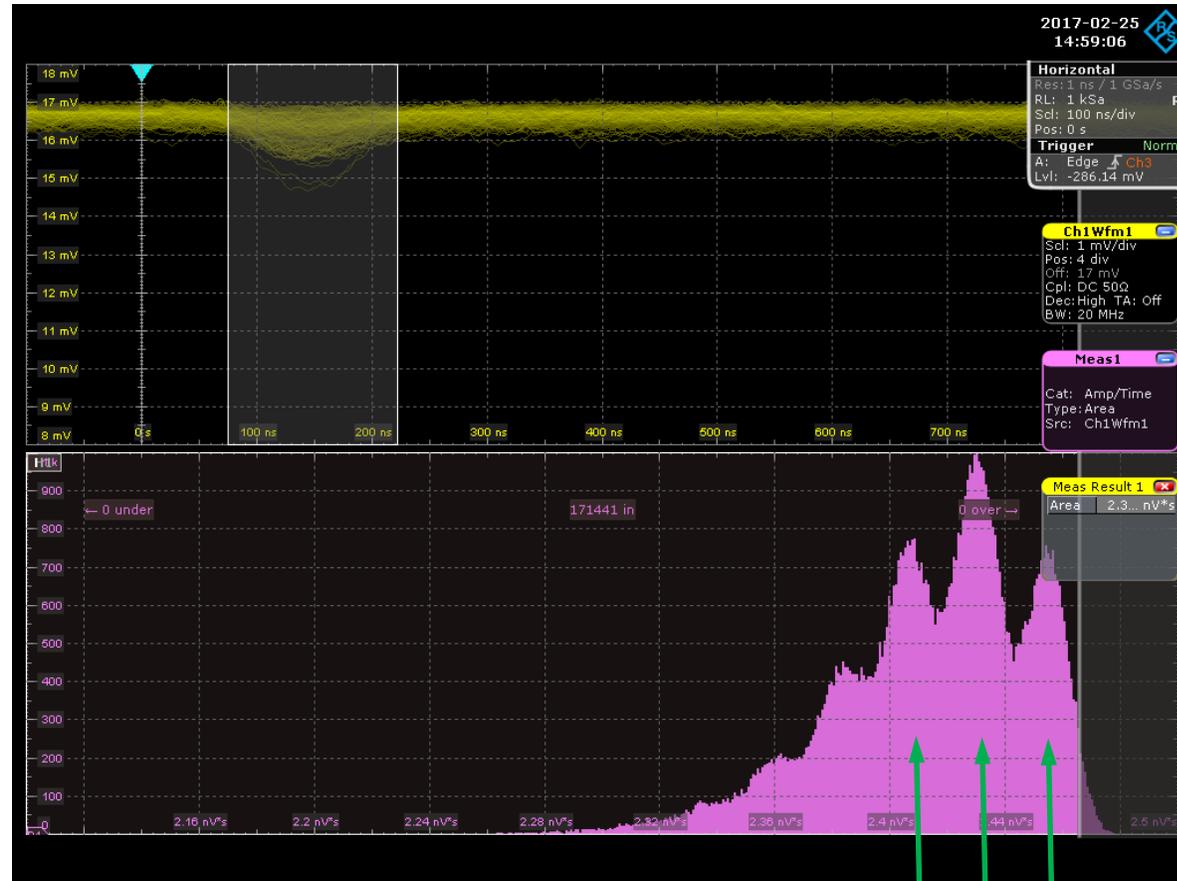


work in progress now



DEP data
(very soon!)

Resolution of **FEE** is sufficient to see single pixel peaks.
This could be useful for calibration, and is certainly a useful diagnostic.
Note that DEP with a 12 bit ADC is not expected to be able to resolve this!



2 pix
1 pix
ped

Q: What is DEP?

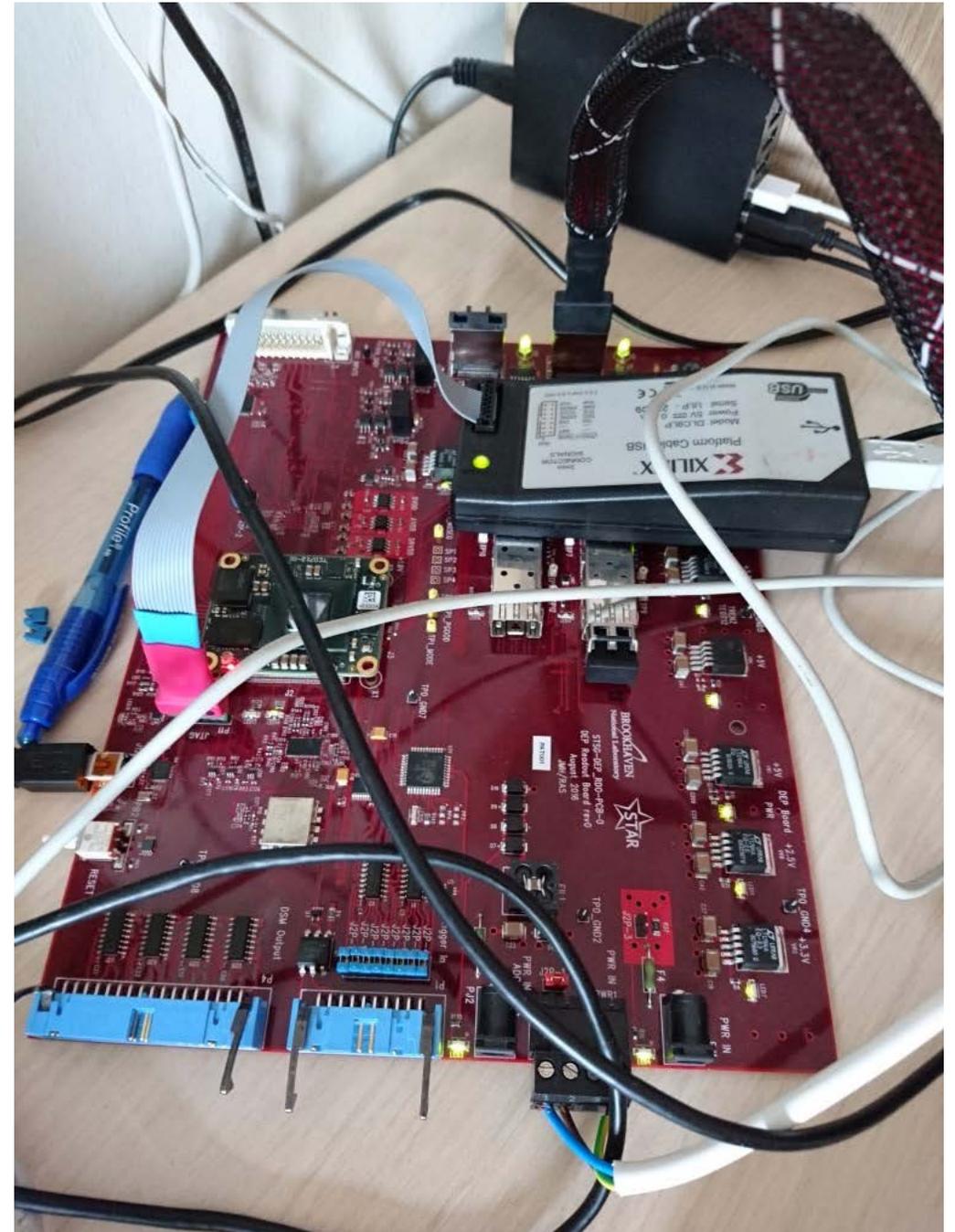
A: DEP is a Concept

- Multi-channel digitizer (16, 32, etc)
- Conceptually a cross between e.g. the QT cards (with timing info) and e.g. the Calorimeter “Tower Digitizers”
 - Direct connection from the detector TCD (for phased RHIC clock, L0 trigger)
 - Direct bidirectional multi-Gb fiber connections to DAQ (as fast as possible)
 - Direct connections to Trigger DSMs (or similar)
 - Direct bidirectional Slow Controls interface to Front End preamplifiers
- ADC is running in oversampled mode at e.g. 8-20X RHIC clock
 - **Not** in integrated (gated) mode!
 - Preamp signal can thus be digitally shaped & manipulated via DSP algorithms
 - Some amount of timing information can thus be extracted via digital algorithms (e.g. center-of-gravity)
 - Increased dynamic range due to oversampling \Rightarrow the total charge is a sum of 8 x 12bit values instead of just 1 x 12 bit value (if integrated)
- Local on-board trigger algorithms using FPGA DSP cores
- As cheap as possible \Rightarrow \$70 per channel (including the DAQ Receiver and PC)
- Compact & self-contained
 - no expensive crates

DEP Prototype (... or the first DEP implementation)

- 16 channel card
 - 8 channels have simple line receivers – direct connection of cable to ADC through AC coupling capacitors
 - 8 channels have more complex “Gerard” receivers
- 12 bit differential ADCs running at 8X RHIC clock (~80 Msps/s)
 - Cheap data cable and connector
- 3.2 Gbit interface to a DAQ Receiver
 - With pedestal subtraction, zero-suppression, maybe tail suppression etc.etc.etc.
 - Lots of pre/post data at full 80 Msps/s for debugging
- Connected to a DAQ TCD for a real, timed & phased RHIC clock
 - Can be externally triggered but can also be self-triggered for debugging & evaluation
- 16 PECL outputs via “standard” DSM cable to a (possible) DSM
 - Trigger algorithms TBD
 - Timing resolution TBD but expect ~1ns
- Slow Controls interface to FEE (a la FPS TUFF) inbuilt into the board
 - Using the same cable/connector as the data ⇒ compact, cheap
- USB interface for debugging and standalone operation
- Enclosure TBD

- Prototype board **installed in STAR**, connected to STAR Trigger & Clock Distribution and readout over fiber. **Tested**.
- Currently in Indiana awaiting further tests with the actual preamplifier
- Firmware under development and will proceed in a few stages
 - basic self-triggered readout mode with pre & post samples
 - basic STAR-triggered readout mode with pre & post samples
 - pedestal subtraction and zero suppression
 - simple trigger algorithms
- Using the Forward Calorimeter prototype we plan to gather significant amount of data to evaluate the concept in this year's Physics run
 - **general response** (signal to noise etc)
 - **timing resolution**
 - **triggering algorithm testbed**



Calorimeter based Triggering

- each DEP board will be capable of local trigger decisions using its 32 channels
 - simple arithmetic e.g. high tower or tower sum but using timing information to suppress the background
- a set of DEP boards (4-5) will combine local trigger primitives
 - e.g. highest tower, various sums
- at which point we can either
 - re-use the current STAR experiment's DSM Trigger boards
 - but very old electronics, maintenance issues, not optimal and some effort to program them
 - make a set of **new electronics boards** specifically tailored to the needs of more sophisticated calorimeter triggers
 - with new generation FPGAs can be made powerful yet cheap and simple
- no decision has been made at this stage of design
 - but is not expected to contribute significantly to the overall system cost