

## EIC Detector R&D Progress Report

**Project ID:** eRD18

**Project Name:** Precision Central Silicon Tracking & Vertexing for the EIC

**Period Reported:** October 1 to December 31, 2019

**Project Leader:** Peter G. Jones

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**Project Members:**

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### Abstract

We propose to develop a detailed concept for a central silicon pixel detector for an Electron-Ion Collider at BNL or JLab exploring the advantages of depleted MAPS (DMAPS) to achieve improved spatial resolution and timing capability over traditional MAPS. The sensor development will exploit the Birmingham Instrumentation Laboratory for Particle Physics and Applications. An accompanying simulation study will optimise the basic layout, location and sensor/pixel dimensions to find the best achievable momentum resolution and vertex reconstruction resolution. This initial design study will allow future full-detector simulations to explore precision measurements of heavy flavour processes and scattered electrons at high  $Q^2$ .

## 1. Past

### 1.1 *What was planned for this period?*

The project is divided into two work packages. WP1 focuses on sensor development and WP2 focuses on detector layout simulations. For this period, the plan for WP1 was to continue the technology investigations into the modified TJ 180 nm CIS process, possibly using new prototypes developed in this technology, and to complete the feasibility study for the design of the pixel and readout architecture for an EIC specific DMAPS sensor. For WP2, we aimed at summarising the basic layout simulations carried out with EICRoot, and to start full-detector simulations to explore precision measurements of heavy flavour processes at high  $Q^2$ .

### 1.2 *What was achieved?*

In this section, we divide our report into sections corresponding to the work packages defined above.

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### 1.2.1 WP1 – TJ technology investigations

In the past six months, the work on technology investigations focused on completing the analysis of the Mini-MALTA Diamond test beam data, resulting in a publication together with collaborators at CERN and Oxford [1]. The Mini-MALTA prototype implements 64x16 pixels with a pitch of 36.4  $\mu\text{m}$ . The pixels are organised in various sectors that differ in sensor layout and front-end design. In particular, three sensor variants are implemented: the sensor design with a continuous deep n-layer implemented in previous MALTA prototype [2] (called MALTA sector in the following), and two new variants called “n-gap” and “extra deep p-well” designs that have a non-continuous n-layer. The new modifications to the sensor layout have been proposed to improve charge collection properties at the pixel edges, where low efficiency has been measured in MALTA test beams [2]. The three different pixel cross-sections are shown in figure 1. TCAD simulations have shown that both solutions bend the electric field lines towards the collection electrode leading to faster charge collection and larger signal from the pixel edge with respect to the MALTA sensor design [3].

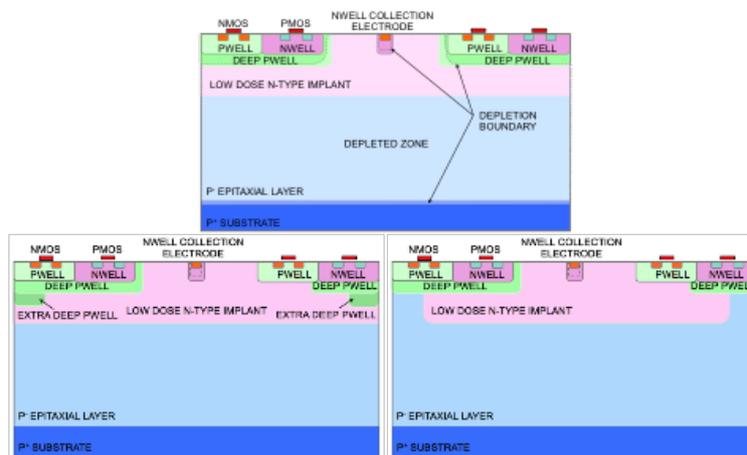


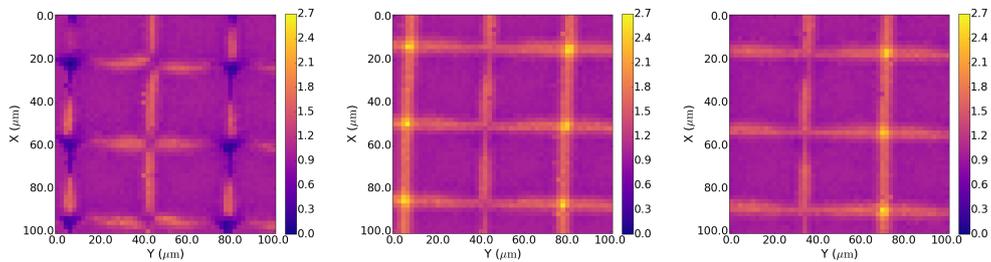
Figure 1: Cross section of the TowerJazz process: continuous n-layer (top), extra deep p-well at the edge of the pixel (bottom left), and low dose n-implant removed (n-gap) at the edge of the pixel (bottom right) [2].

The test beam was performed at the Diamond Light Source using a micro-focus 8 keV X-ray beam. The beam was scanned across the surface of the device in 2  $\mu\text{m}$  steps. Both un-irradiated and irradiated sensors were tested. Scans were performed for different bias voltages. The in-pixel response to photons was determined from the number of hits in each pixel at each stage position [1].

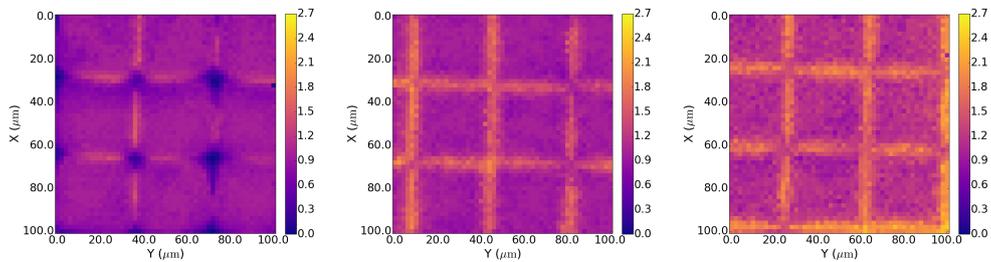
The pixel response map for the three different sectors is shown in figure 2. Sectors from un-irradiated and irradiated sensors are compared for the same bias voltage of -6 V on the p-substrate and p-well. Before irradiation, the MALTA sector shows a uniform response in the centre of the pixel, which degrades at the corners. After irradiation, the pixel response at the edges and in the corners decreases significantly, as expected from the test beam results presented in [2]<sup>2</sup>. The modified sensor layouts

<sup>2</sup> The asymmetric response at the edge of the pixel in the MALTA is due to physical implementation of the deep p-well. Further details can be found in [1].

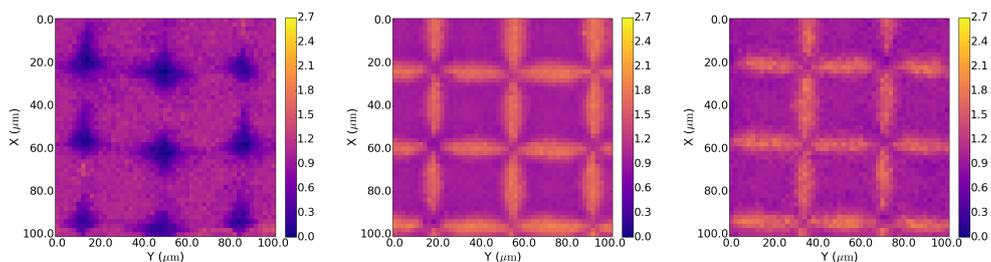
demonstrate an improved performance. Before irradiation the response in the middle of the pixel is comparable to the one in the MALTA sector, but there is a significantly improved performance at corners and along the edges of the pixels. After irradiation (up to  $1e15$   $1$  MeV  $n_{eq}/cm^2$ ), the modified sectors maintain a good response overall, with only a small decrease at the corners.



(a) W2R11 MALTA, unirradiated (b) W2R11 pwell, unirradiated. (c) W2R11 ngap, unirradiated.



(d) W2R9 MALTA,  $5e14$   $n_{eq}/cm^2$ . (e) W2R9 pwell,  $5e14$   $n_{eq}/cm^2$ . (f) W2R9 ngap,  $5e14$   $n_{eq}/cm^2$ .

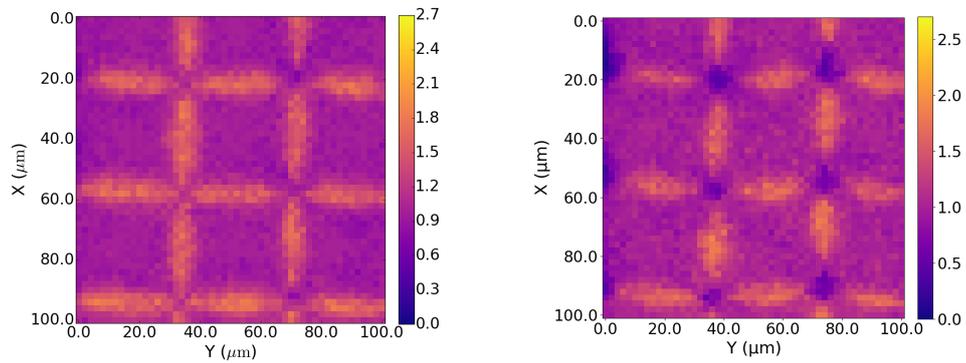


(g) W2R1 MALTA,  $1e15$   $n_{eq}/cm^2$ . (h) W2R1 pwell,  $1e15$   $n_{eq}/cm^2$ . (i) W2R1 ngap,  $1e15$   $n_{eq}/cm^2$ .

Figure 2: Pixel response for MALTA sector (left column), extra deep p-well sector (middle column), and n-gap sector (right column). W2R11 is un-irradiated, W2R9 is irradiated with protons to  $5e14$   $1$  MeV  $n_{eq}/cm^2$ , and W2R1 is irradiated with neutrons to  $1e15$   $1$  MeV  $n_{eq}/cm^2$  [1].

Figure 3 compares the performance of the sector with n-gap modification irradiated to  $1e15$   $1$  MeV  $n_{eq}/cm^2$  for a voltage of  $-6$  V and  $-20$  V applied to the p-substrate. For an increased sensor bias voltage, the pixel response decreases at the corners. A higher bias voltage works against the modifications, shaping the electric field lines at the pixel

edge such that charges in these areas drift vertically below the p-well and then laterally along a longer drift path towards the collection electrode.



(a) N-gap sector in W2R1 at -6 V biasing voltage.

(b) N-gap sector in W2R1 at -20 V biasing voltage.

Figure 3: Pixel response for the n-gap sector in sensor W2R1 (irradiated with neutrons to  $1e15$   $1 \text{ MeV } n_{eq}/\text{cm}^2$ ), for different bias voltages [1].

The average pixel response for the different sectors before and after irradiation, and for the different bias configurations is summarised in table 1 and 2, showing the better response from the modified sectors due to the more uniform charge collection.

Table 1: Average pixel response for the three sectors in irradiated and n-irradiated sensors [1].

Sample	Fluence $n_{eq}/\text{cm}^2$	TID (MRad)	MALTA response (%)	p-well response (%)	n-gap response (%)
W2R11	0	0	$88.3 \pm 2.4$	$90.5 \pm 2.2$	$90.9 \pm 2.2$
W2R9	$5e14$ (p)	66	$81.2 \pm 2.8$	$87.6 \pm 4.2$	$88.4 \pm 3.8$
W2R1	$1e15$ (n)		$75.4 \pm 3.8$	$90.5 \pm 2.8$	$89.0 \pm 3.1$
W5R9	$5e14$ (p)	70	$80.4 \pm 2.8$	$89.0 \pm 2.5$	$89.3 \pm 2.2$
W4R9	$7e13$ (p)	9	$78.7 \pm 2.6$	$89.8 \pm 2.3$	$89.9 \pm 2.3$

Table 2: Average pixel response for the three sectors in sensor W2R1 (irradiated with neutrons to  $1e15$   $1 \text{ MeV } n_{eq}/\text{cm}^2$ ), for different bias voltages [1].

Sample	Bias (V)	MALTA response (%)	p-well response (%)	n-gap response (%)
W2R1	-6	$76.7 \pm 3.8$	$91.1 \pm 3.0$	$90.0 \pm 3.1$
	-20	$72.2 \pm 3.3$	$86.6 \pm 3.9$	$86.4 \pm 2.9$

These results show that the proposed further modifications of the TJ 180 nm CIS process improve the electric field configuration and thus lead to better charge

collection properties. The optimal bias configuration is found with -6 V on the p-substrate and p-well.

### *1.2.2 WP1 – EIC-specific sensor development*

The main focus of WP1 at present is a feasibility study into the design of an EIC specific DMAPS sensor. This study is carried out in collaboration with a chip designer at RAL and looks at options for the pixel design and readout architecture that would match the requirements for a tracking and vertex detector at an EIC, with the added capability to time stamp individual bunch crossings. The specifications derived from previous technology investigations and detector simulations are shown in Appendix 1. The study tries to find solutions to design one DMAPS sensor that could be used both for vertex and tracking, and time stamping. Should the required time resolution for time stamping require a prohibitive power consumption and pixel size for use in the vertex and tracking detector, a dedicated sensor would be required to be used in a time stamping layer placed at the outermost radius, before the TPC. For this layer requirements on pixel size and power consumption (i.e. material budget) can be significantly relaxed without compromising tracking performance.

In the past six months, we concluded the first part of the feasibility study, i.e. the pixel design. Results are summarised here and will be presented in full in the report to be submitted to the panel upon completion of the study. More details will be given as well in the talk at the advisory committee meeting in January.

Timing performance in traditional pre-amp and comparator pixel designs is affected by two main factors: time walk, and jitter due to noise in the circuit. Simulations of the ALPIDE front-end showed that this would have a time walk of 700 ns for charges between 0.5ke<sup>-</sup> and 2.5ke<sup>-</sup>. Transient noise simulations showed that the hit time response variation after the comparator would be around 30 ns for the leading edge and almost 200 ns for the trailing edge, for the same charge.

Time walk can be corrected and various mechanisms exist for this. Two methods have been investigated in this study: constant fraction discrimination (CDF), and a calibration method based on measurement of Time-Over-Threshold (TOT) and Time-Of-Arrival (TOA), that is the approach adopted by the TimePix chip [5]. Other methods have been considered, such as those implemented in the in MuPix chip [6] and FE-I4 chip [7], but these have not been investigated as the time resolution they achieve is not sufficient for our case study.

Noise performance improvement however requires higher power. Figure 4 shows the simulated analogue output of a simple common source amplifier used as pixel front-end, for various bias currents. This simulation shows that the time resolution required to time stamp hits at an EIC is not possible within the power specifications of the vertex and tracking detector for a traditional pixel architecture, and a sensor with higher power consumption would be needed to deliver this time resolution in a dedicated time stamping layer. Simulations of traditional pixel architectures with CDF or TOT/TOA calibration method have been made, including transient noise and process variation, to quantify pixel size and power density for such a sensor.

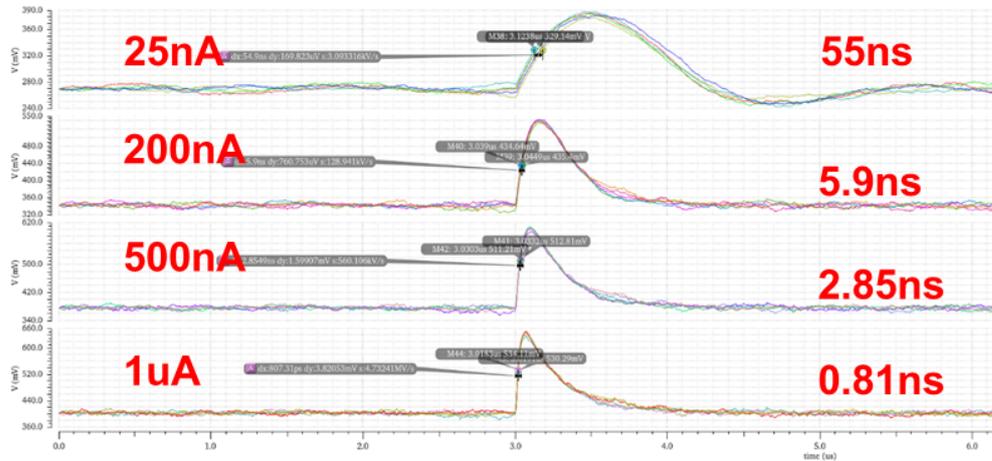


Figure 4: Timing jitter for a common source front-end for different value of the amplifier bias current.

**TOT/TOA calibration method:** Simulations for the TOT/TOA calibration method have been made with a traditional pre-amp, shaper, comparator geometry. Simulations have been made to study the variation of TOA and TOT with hit size. From these a plot of TOT versus TOA can be made to determine the precision required for the measurement of the leading and trailing edges in order to be able to apply the time walk calibration mechanism. This is shown in figure 5. The figure highlights as an example that to achieve the more challenging time resolution of 1 ns on the leading edge, the TOT can be measured with a precision of 8 ns.

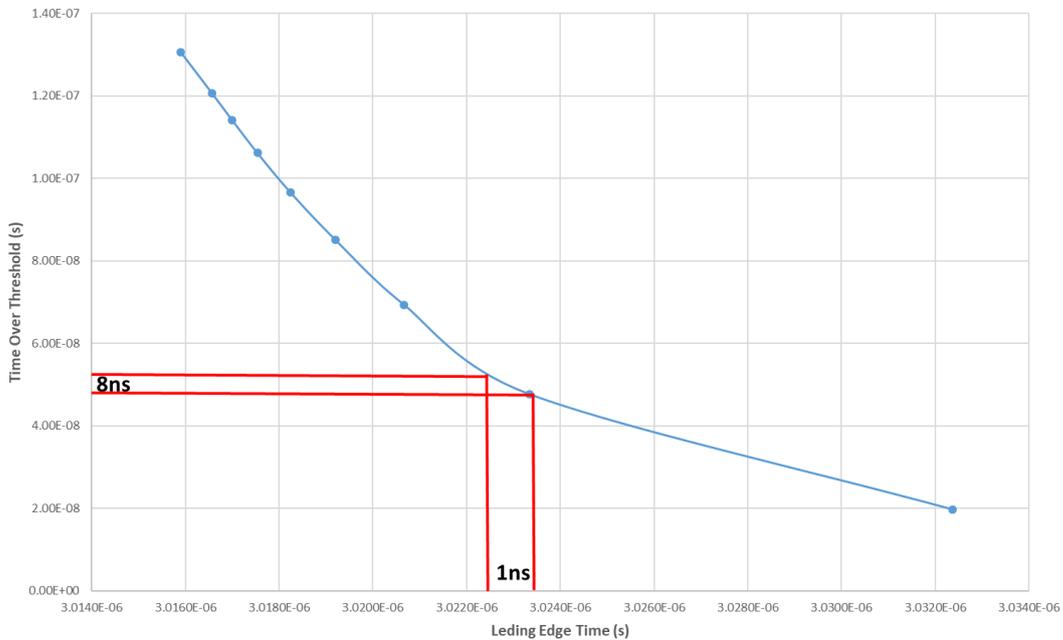


Figure 5: TOT versus leading edge (i.e. TOA) for a pre-amp, shaper, comparator pixel front-end design.

Knowing the precision required for the leading and trailing edge, we evaluated whether the pixel has sufficient noise performance to meet these requirements. This

was done by running transient noise simulations on the pixel design and measuring the variation of the reported ToA and ToT times. Results are shown in table 3 for three different charges. The noise performance of this architecture would seem sufficient for the required time resolutions, within 5 sigma for the 10 ns case.

Table 3: Standard deviation of TOA and TOT measured from 500 transient noise simulations runs for three different hit sizes.

Hit Size (e-)	ToA Standard Deviation (ps)	ToT Standard Deviation (ns)
500	429	2.45
750	278	3.21
2500	130	2.35

Finally, the power density for different pixel sizes has been measured in simulations. As anticipated, this approach would require the design of a sensor for a dedicated time stamping layer, as the power consumption would be prohibitive in the 20  $\mu\text{m}$  pixel of the vertex and tracking layer. The power consumption specification for the timing layer (200  $\text{mW}/\text{cm}^2$ ) could be met with a pixel pitch of 90  $\mu\text{m}$ . For the maximum pixel pitch specified for this layer (350  $\mu\text{m}$ ), the power consumption would be below 20  $\text{mW}/\text{cm}^2$ .

**Constant fraction discriminator:** A typical CDF architecture has been simulated showing that the time walk for hit sizes in a range between 0.5ke- and 2.5ke- would be less than 4 ns. Transient noise simulations showed that for the same range of hit sizes, the maximum spread of recorded hit time would still be below 4 ns, with a standard deviation of 400 ps, matching the requirement for the 10 ns time resolution case. This approach could not provide the 1 ns time resolution for an EIC at JLAB.

For this specific architecture, the effect of process variation has also been considered as this design is dependent on the relationship between the attenuated and delayed signal paths. The results showed that the effect of process variation would significantly increase the tail of the distribution to above 10 ns, rendering this approach unusable for both EIC implementations. This approach is thus not considered as an option for our application.

Based on these results a different route is being explored looking into an alternative low power front-end architecture (LPFE) for the TOT/TOA calibration method. The idea is to try and match the requirements on time resolution and power consumption simultaneously. A front-end architecture derived from the ALPIDE FE is being simulated. Preliminary results show that one sensor with a pixel pitch of 20  $\mu\text{m}$  could be designed that with different FE bias currents could achieve the 10 ns, and possibly 1 ns resolution. The resulting power density for the 10 ns resolution would be within the specifications of the vertex and tracking detector so that time-stamping capability could be added to all layers. For the 1 ns resolution the power consumption will be higher, but well within the specifications for a timing layer. Still the same chip could

be used everywhere with different configurations. A low FE bias current configuration would be used in the innermost vertex and tracking layers, and a configuration with higher FE bias current would be used in the outermost layer to time stamp hits. This architecture is potentially very promising, but it comes with some caveats on the minimum detectable signal. The full results will be presented at the advisory committee meeting in January.

### *1.2.3 WP2 – Detector layout simulations*

In the past six months, work on simulations has focused on basic layout simulations in EICROOT of an all silicon vertex and tracker detector, where the TPC is replaced by silicon barrel layers and disks.

A summary of the basic layout simulations carried out within WP2 is currently being finalised and will be submitted in time for the January meeting. It will include baseline performance plots obtained using EICROOT for both the central and forward regions of a silicon plus TPC tracker and initial investigations of an all-silicon tracker design.

With the help of Yulia Furletova and collaborators at JLab, Håkan Wennl f has now successfully migrated his simulation setup from EICROOT to the G4E framework, and is ready to start heavy flavour physics simulations. The G4E framework offers greater flexibility than EICROOT and is one of the two simulation frameworks supported by the Software Consortium for the upcoming Yellow Report design studies.

### *1.3 What was not achieved, why not, and what will be done to correct?*

The feasibility study has not yet been completed. As the study into the pixel design progressed, more options than originally planned were identified that were interesting to investigate. In addition, in order to move to the next part of the study covering the readout architecture, more information is needed to define specifications that is not yet available, the most important one being the hit occupancy. Whilst we do not expect the hit occupancy due to physics events to be an issue, occupancy due to hits from synchrotron radiation can be significant. The beam-related background is difficult to estimate as it depends on the details of the IR design, in particular the placement of collimators. We hope to obtain estimates of the beam background from the simulation studies being performed by eRD21. We will also make rough estimates informed by the experience of H1 at HERA.

## **2. Future**

### *2.1 What is planned for the next funding cycle and beyond? How, if at all, is this planning different from the original plan?*

The plan for the remaining six months is to conclude this initial R&D phase, and to prepare for future work that would lead to a prototype DMAPS sensor meeting the EIC specifications.

We believe that at this stage the investigations on the TJ 180 nm CIS technology are fairly complete, so the work will concentrate on the feasibility study. We aim at finishing the feasibility study with investigations of possible readout architectures in

the remainder of FY20 and have a final report ready to be submitted to the panel with the project report and proposal in July 2020. Our next proposal for FY21 will present the course of the second phase of the project towards an EIC sensor prototype.

With the basic layout simulations completed and summarised, and the G4E simulation framework installed and running, work can commence on physics performance simulations. Initially the G4E simulation framework will be benchmarked against EICROOT. Then, physics simulations will start with focus on reconstruction of charm mesons, such as the  $D^{*+}$  and  $D^0$ . This work will feed into the Detector/Physics Working Group input into the EIC Detector Yellow Report.

## 2.2 *What are the critical issues?*

See section 1.3.

## 3. Personnel

*Include a list of the existing personnel and what approximate fraction each has spent on the project. If students and/or postdocs were funded through the R&D, please state where they were located and who supervised their work.*

Prof. Peter Jones (0.05 FTE) – no cost

Dr. Laura Gonella (0.1 FTE) – no cost

Håkan Wennlöf – (1 FTE) – no cost

Prof. Phil Allport and Prof. Paul Newman have an advisory role and participate in our regular project meetings to monitor progress.

## 4. External funding

*Describe what external funding was obtained, if any. The report must clarify what has been accomplished with the EIC R&D funds and what came as a contribution from potential collaborators.*

The University of Birmingham provides the Ph.D. studentship that supports Håkan Wennlöf. In addition, our bid to support some of the R&D elements of this proposal through EU Horizon 2020 has been successful. This formed part of the NextDIS work package included in the STRONG-2020 proposal. The proposal has been awarded €62.5k to support the submission of an EIC DMAPS sensor prototype.

## 5. Publications

*Please provide a list of publications coming out of the R&D effort.*

None at this stage of the project.

## 6. References

- [1] M. Mironova et al., *Measurement of the relative response of TowerJazz Mini-MALTA CMOS prototypes at Diamond Light Source*, arXiv:1909.08392.
- [2] R. Cardella et al, *MALTA: an asynchronous readout CMOS monolithic pixel detector for the ATLAS High-Luminosity upgrade*, 2019 JINST 14 C06019.
- [3] M. Munker et al, *Simulations of CMOS pixel sensors with a small collection electrode, improved for a faster charge collection and increased radiation tolerance*, 2019 JINST 14 C05013.
- [4] K. Moustakas et al., *CMOS Monolithic Pixel Sensors based on the Column-Drain Architecture for the HL-LHC Upgrade*, NIM A936 (2019) 604-607, <https://doi.org/10.1016/j.nima.2018.09.100>
- [5] T. Poikela et al., *Timepix3: a 65K channel hybrid pixel readout chip with simultaneous ToA/ToT and sparse readout*, 2014 JINST 9 C05013, <https://doi.org/10.1088/1748-0221/9/05/C05013>
- [6] H. Augustin et al., *MuPix8 — Large area monolithic HVCMOS pixel detector for the Mu3e experiment*, NIM A936 (2019) 681-683, <https://doi.org/10.1016/j.nima.2018.09.095>
- [7] M. Garcia-Sciveres, *The FE-I4 pixel readout integrated circuit*, NIM A636 (2011) S155-S159, <https://doi.org/10.1016/j.nima.2010.04.101>

## 7. Appendices

### Appendix 1

Table A.1: Updated specifications for an EIC DMAPS detector. Two sets of specifications are collected, one for the vertex and tracking detector without timing capability, and one for a timing layer with capability to tag bunch crossings.

	<b>EIC DMAPS Sensor</b>	
<b>Detector</b>	Vertex and Tracking	Added time stamping
<b>Technology</b>	TJ or similar	
<b>Substrate Resistivity [kohm cm]</b>	1	
<b>Collection Electrode</b>	Small	
<b>Detector Capacitance [fF]</b>	<5	
<b>Chip size [cm x cm]</b>	Full reticule	
<b>Pixel size [<math>\mu\text{m} \times \mu\text{m}</math>]</b>	20 x 20	max 350 x 350
<b>Integration Time [ns]</b>	2000	
<b>Timing Resolution [ns]</b>	<i>OPTIONAL</i> < 9 (eRHIC) < 1 (JLEIC)	< 9 (eRHIC) < 1 (JLEIC)
<b>Particle Rate [kHz/mm<sup>2</sup>]</b>	<b>TBD</b>	
<b>Readout Architecture</b>	Asynchronous	<b>TBD</b>
<b>Power [mW/cm<sup>2</sup>]</b>	<35	<200
<b>NIEL [1MeV neq/cm<sup>2</sup>]</b>	10 <sup>10</sup>	
<b>TID [Mrad]</b>	< 10	
<b>Noise [electrons]</b>	< 50	
<b>Fake Hit Rate [hits/s]</b>	< 10 <sup>-5</sup> /evt/pix	
<b>Interface Requirements</b>	<b>TBD</b>	