Letter of Intent for EIC Detector R&D

Title: Low-Mass Silicon Pixel Sensor with In-Pixel Readout Electronics for EIC Tracking and Vertexing

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Collaboration:
We expect to collaborate with several institutes in the EIC detector R&D community, including the groups on silicon R&D at LBNL (eRD16), University of Birmingham (eRD18), JLAB (eRD22), and ANL; and potentially the consortia on tracking (eRD6), calorimeter (eRD1), and PID (eRD14), upon further discussion.

Upon recognizing the importance of the EIC project to U.S. nuclear science, and the need on developments in many areas beyond the present state-of-the-art in detector technology, we propose a generic R&D project involving low-mass silicon pixel sensors with in-pixel readout electronics for EIC tracking and vertexing, based on the extensive studies that have been carried by the EIC detector R&D community.

As the current main-stream HEP and NP R&D is mainly related to LHC Phase-I (ALICE and LHCb) and Phase-II upgrade (ATLAS, CMS), which focus on radiation hardness and high-rate capabilities, many requirements for an EIC are not covered and there is a need to develop technologies to fulfill tasks unique to an EIC [1]. For the vertex tracker, the most promising technology is likely Monolithic Active Pixel Sensors (MAPS) based on CMOS technology, to meet the required spatial resolution, readout speed, and material budget [1-2]. The ALPIDE chip [3], developed at CERN with collaborators for ALICE, has a major advantage of integrating both active pixel sensor and in-pixel readout electronics (amplification and discrimination) within the 30um x 30um pixel area in a commercial CMOS image process (TowerJazz 180nm), thus maintaining the spatial resolution at a very low material budget. However, since the charge is collected mainly by diffusion in the epitaxial layer, a major issue is charge loss by trapping. Several other state-of-the-art MAPS technologies (e.g. DMAPS, HV CMOS, HV SOI, and DEPFET), focus on improving the sensor signal-to-noise-ratio and the radiation hardness through depletion, all requiring external readout ASICs, which therefore increases the material significantly.

Motivated by requirements of low mass, high spatial resolution and readout speed for an EIC, we propose to develop a new technology, based on a commercial deep sub-micron Silicon-On-Insulator (SOI) process, to make a low-mass silicon pixel sensor with in-pixel readout electronics for EIC tracking and vertexing. Deep submicron technologies have been shown to provide greater radiation hardness than coarser technologies. SOI has the advantage that the device layer can be very thin with the active silicon layer of only a few micrometers, limiting the material budget and the associated multiple Coulomb scattering; and the bulk of the wafer below the active layer is electrically isolated from this active layer so electrons scattered into that region do not degrade the image. One possibility is to etch off the entire handling wafer (~50 um), and use the buried oxide layer (SiO2) as a strong supporting material and as a natural etching stopper for uniformity, achieving much lower mass than the state-of-the-art MAPS technologies. Integrating sensor with in-pixel readout electronics is essential to reduce the mass of external readout ASICs. Developing low-noise front-end amplification, shaping, and discrimination with 10~20 transistors in ~20~30um pitch is very challenging. The use of deep sub-micron design rules also means that
smaller pixels are possible, and the lower capacitances involved suggest that lower noise and higher speed readout should be possible. The target shaping time is less than a few tens of ns, in order to differentiate between particle bunches [1-2]. To achieve the lower noise and faster shaping than what has been achieved in ALPIDE, higher analog power than 40nW/pixel in ALPIDE would be necessary. This is possible since 90% of the total power (~40 mW/cm²) in ALPIDE was allocated to common digital processing; the power budget for an EIC tracker needs to be specified.

We plan for the next several months some initial experiments to test the concept, which includes: test the low-mass SOI concept on commercial SOI wafers, currently in collaboration with X-FAB; develop and characterize different photodiode architectures (within a few um) on thinned SOI wafer and measure dark current in Instrumentation’s clean room; develop in-pixel readout electronics upon selected SOI technology in Instrumentation’s Microelectronics group; characterize prototype low-mass sensor with in-pixel readout electronics with beam sources, in collaboration with the EIC community.

We will need close collaboration with the EIC community for inputs of detector specifications to optimize the sensor and electronics design to achieve low noise, fast readout at very low power. Especially, we hope for frequent conversations with the EIC silicon groups [4-7] for technical discussions and exchanges of R&D results to proceed efficiently. Currently we are also collaborating with BNL NSLS-II for Cryo-Electron Microscopy & Ultrafast Electron Diffraction experiments, on testing the low-mass SOI concept.

The Instrumentation Division, in the Nuclear and Particle Physics directorate, has been developing detectors and fast electronics for high energy and nuclear physics experiments for a number of years, with the goal of making precision measurements of position, time, and energy of ionizing particles, and setting the standard for state-of-the-art performance. Front-end electronics forms an integral part of the detection system, and we devote significant effort to co-developing optimal signal processing for each detector that has been developed. This project draws upon decades of experience at BNL in detector and instrumentation development and it leverages state-of-the-art ASIC development expertise, as well as material characterization capabilities provided by the National Synchrotron Light Source-II and the Center for Functional Nano-materials.