



Submitted June 16, 2017

## Proposal to Investigate Silicon CMOS

**Whitney Armstrong**, Argonne National Laboratory

**David Blyth**, Argonne National Laboratory

**Jessica Metcalfe**, Argonne National Laboratory (principal investigator and contact person)

**José Repond**, Argonne National Laboratory (co-principal investigator)

**Junqi Xie**, Argonne National Laboratory

**Abstract:** This is a new proposal to investigate silicon CMOS technologies as a stepping stone toward an Ultra-Fast Silicon Detector implemented in a CMOS process. This initiative is part of a larger effort by the Argonne EIC collaboration to develop an alternative detector solution for the EIC, which utilizes Ultra-Fast CMOS in both a tracker and electromagnetic calorimeter of an EIC detector. Through the precise measurement of the time-of-flight of charged particles, such silicon sensors would provide particle identification (pion – kaon – proton separation) for most of the solid angle of a  $4\pi$  detector and would thus eliminate the need of dedicated particle identification systems (e.g. Cerenkov detectors) placed in front of the calorimeter. High performance particle identification is required for precision measurements of transverse momentum dependent parton distributions (TMDs), as well as of heavy flavor production in deep inelastic scattering and the related charm and beauty parton distributions.

## 1. Physics motivation

The measurement of key physics processes, such as semi-inclusive deep inelastic scattering and charm production require particle identification, i.e. the separation of pions, kaons, and protons [1]. (The identification of electrons is typically achieved through the measurement of the associated shower shape and the charged track momentum.) Traditionally, particle identification is obtained from dedicated subsystems, e.g. Cerenkov or Time-of-flight counters. For best performance, these need to be placed in front of the calorimeter, thus increasing the amount of material in front of the calorimeter and in turn degrading latter's performance.

We propose an alternative way to achieve particle identification by introducing precise timing into the silicon sensors of both the (vertex and outer) tracker and the electromagnetic calorimeter. This approach eliminates the need of additional particle identification sub-systems and simplifies the concept of a general  $4\pi$  detector. The advantages to this approach are many:

- Simplification of the detector concept by eliminating now redundant sub-systems
- Significant reduction of inert material in front of the calorimeters
- Improved reconstruction (efficiency, energy and angle) of photons in the calorimeter
- Improved kinematic reconstruction, in particular for charged current events.

The proposed work is equally applicable to a detector destined for eRHIC or JLEIC.

## 2. Required timing resolution

The requirements on the timing resolution for sensors were studied based on a complete simulation of the concept of an EIC detector. The simulation is based on GEANT4 and includes all relevant systems of a generic  $4\pi$  detector: a five-layer silicon vertex detector, a five-layer silicon outer tracker, a 20-layer electro-magnetic calorimeter with silicon sensors and tungsten absorber plates, and a hadron calorimeter (not used in this analysis). The energy deposits in the active media of the detector were digitized to emulate the performance of a realistic device. The position and exact time, as provided by GEANT4, were recorded for each hit.

The aim of the study was to determine the requirements on the timing resolution for particle momenta up to seven GeV/c, the range of momenta for particles reaching the barrel and most of the area covered by the forward detectors. Single particles (pions, kaons, and protons) were generated spanning the entire barrel region. In order to establish the timing requirement, the hit times in the sensors were smeared with a Gaussian with a fixed width ranging from zero to 30 picoseconds. After the smearing, the times versus flight paths were fitted with a linear function to determine the speed of the particle. The mass of the particle was reconstructed using both the measured momentum (from the track fit) and the reconstructed speed of the particle. As an example, Fig.1 shows the reconstructed mass for the kaon sample with hit times smeared by ten picoseconds.

In the following, pions (kaons) are identified as particles with a mass smaller (larger) than  $400 \text{ MeV}/c^2$ . The resulting kaon identification efficiency and pion contamination are shown in Fig.2 as a function of track momentum and again with a ten picosecond smearing of the hit times. The study concludes that a ten picosecond resolution provides the necessary efficiency and purity for pion/kaon separation (>85% up to  $7 \text{ GeV}/c$ ). Due to the slower velocity of protons, this method enables the separation of protons from kaons with near 100% efficiency.

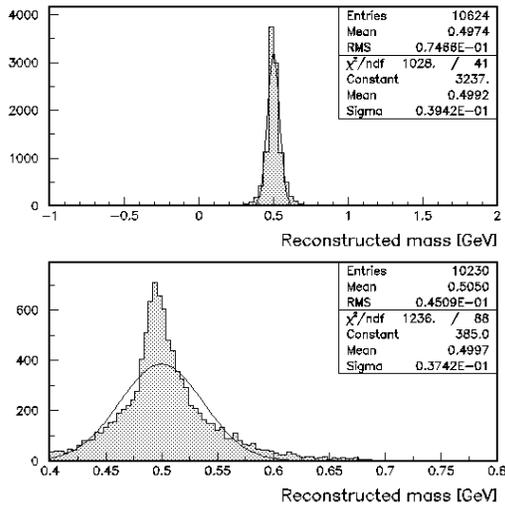


Figure 1. Reconstructed mass of kaons in the barrel region of the SiD detector with hit times smeared by 10 picoseconds.

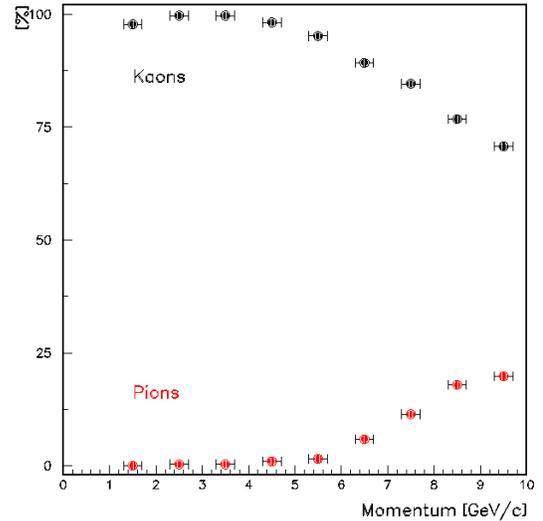


Figure 2. Efficiency for kaon identification and pion contamination established with samples of equal size. The hit times were smeared by 10 picoseconds.

### 3. Proposal

The ultimate aim of the ANL EIC silicon detector program is to use an ultra-fast CMOS detector for the tracker and electromagnetic calorimeter as motivated in the previous section. This proposal aims to advance CMOS technology towards an EIC specific design that fulfills the timing requirements. Current CMOS timing is of the order of 100 nanoseconds [2,3] and insufficient for particle identification at the EIC. As CMOS technology advances, we will focus on the timing characterization of existing technologies with the aim of optimizing timing precision for EIC applications.

The pathway for this development requires a fully monolithic CMOS design optimized for the EIC, followed by the implementation of an ultra-fast gain layer [4,5]. To achieve this goal, we plan to take advantage of the ongoing CMOS R&D program at ANL in collaboration with the University of Geneva, Karlsruhe Institute of Technology, Brookhaven National Laboratory, and the University of Liverpool, among others. This team is looking at the AMS foundry CMOS options designed by Ivan Peric [6] for the Inner Tracker (ITK) Pixel upgrade of ATLAS [7].

This proposal plans to leverage complimentary work at Argonne National Laboratory (ANL). As part of a Lab Directed R&D (LDRD) project, ANL is executing a multi-pronged initiative to contribute to the EIC effort through theoretical studies, Geant4 [8] detector simulations, detector R&D, and accelerator studies. One initial result of this program is the justification for the pursuit of an ultra-fast silicon detector as shown in Section 2. Further studies will be performed in this vein as part of the LDRD program and are not included in this proposal. These include timing synchronization of sensors over the whole detector and testing of current ultra-fast silicon detector (UFSD) technologies.

#### 4. CMOS Sensors

CMOS technology is under investigation for a number of particle physics applications including ATLAS, CLIC, Mu3e, etc. A CMOS pixel is characterized by having circuitry directly on top of the pixel diode structure isolated by a deep well. One implementation is to have a preamplifier on-pixel that is capacitively coupled to a read-out chip. In a fully monolithic design the on-pixel electronics can include full digitization before the signal is transmitted to the periphery. The advantages of a fully monolithic CMOS detector include high pixel granularity, large signals, fast rise time, reduced material, large production capacity, minimal inactive areas, and reduced cost.

There are several ongoing design efforts for CMOS detectors categorized by the design team and the foundries used for fabrication. The AMS foundry has the capability to implement an HV process enabling up to 120 V and to use high-resistivity p-type wafers in both 180 nm and 350 nm nodes. The drawback with the AMS foundry is that there is no way to isolate the n-wells from the collecting deep n-well limiting the options for CMOS electronics on the pixel. CMOS technologies from other foundries such as TowerJazz and L-Foundry have their own distinct advantages and disadvantages and are being explored by the EIC group at the University of Birmingham. This proposal and the program at Birmingham compliment each other by investing in different approaches for an EIC CMOS detector. While work from this proposal aims to achieve 10 ps timing in CMOS, it can be noted that a CMOS technology used for tracking and vertexing alone would benefit an EIC detector.

The H35demo [9] is implemented in the AMS 350 nm node with  $50\ \mu\text{m} \times 250\ \mu\text{m}$  pixel size to match the FEI4 readout chip. The two chips are glued together to create a capacitively coupled sensor. Two analog and two digital matrices were implemented in the design as well as four resistivities ranging from  $20\ \Omega\cdot\text{cm}$  to  $1\ \text{k}\Omega\cdot\text{cm}$ . Additional variations include sensors thinned to  $100\ \mu\text{m}$  and backside-bias voltage, which provides a more uniform electric field and better charge collection. Early results indicate full depletion around -40 V, a >99% tracking efficiency, and radiation tolerance beyond  $10^{15}\ 1\ \text{MeV}\ n_{\text{eq}}/\text{cm}^2$ . [3] We plan to investigate the various flavors of the H35demo as well as samples from other AMS submissions, like the recent one in January 2017 in the 180 nm node, with the aim of understanding the optimal parameters for an EIC-specific design.

## 5. Proposed studies

The main objective of this proposal is to take advantage of existing AMS CMOS sensors and to characterize the samples and identify key design features, which will be exploited to optimize the detector for the EIC. For example, each analog matrix is subdivided into different transistor designs that either optimize gain or radiation tolerance through enclosed-layout-transistor geometries. For an EIC detector, radiation tolerance should not be an issue given the low levels expected [10] and designing for a higher gain would be more beneficial.

Additionally, we plan to focus on timing characterization measurements taking advantage of the planned purchase of a femtosecond laser and oscilloscope for the timing synchronization effort. These measurements will be compared to TCAD simulations to establish the timing accuracy of the simulations.

The final step intended for this proposal is to optimize an existing CMOS design in terms of layout and geometry to improve the timing. If funding permits, then in the following year we will submit the EIC design in a multi-project wafer run.

## 6. Budget Request

The nominal budget request is for support of a full-time postdoc to be supervised by J. Repond and J. Metcalfe. The postdoc will be located at Argonne. The funding request is for a fully burdened postdoc salary of \$125,000. The deliverables over the first year are listed below.

### Deliverables:

- 1) The postdoc will carry out test bench measurements in the lab at Argonne as well as test beam measurements at Fermilab and/or CERN. These include:
  - a. Characterization of design options for an EIC
  - b. Precision timing measurements of charge collection properties
  - c. Test beam performance measurements with particle species and energies specific to the EIC
- 2) The postdoc will also perform TCAD simulations using an existing license at Argonne.
  - a. TCAD simulations of existing samples will be set up at Argonne
  - b. TCAD simulation results will be compared to measurements
  - c. An iterative process will aim at identifying the underlying cause of any discrepancies and the simulation will be corrected
- 3) The postdoc will work with our collaborating design engineers to identify modifications in simulation toward a design optimized for timing precision at the EIC.

The third item requires consultation with a design engineer. A budget of \$30,000 is allocated for their time. This person will nominally be Ivan Peric or one of his design team members and will be

located off-site at their institution. It is estimated that the budget for this design engineer could amount to 20% of an FTE depending on their level of experience.

**Budget Scenarios:**

- The nominal budget will complete all three deliverables in the first year.
- The nominal budget minus 20% will complete deliverable items 1-2 since the third item requires compensation for a design engineer and this funding would be dropped first.
- The nominal budget minus 40% will complete only the first deliverable using 0.75 FTE of the postdoc the other 0.25 FTE would be funded for different work under the EIC LDRD program.

Budget Scenarios	Postdoc Salary (\$k)	Design Engineer (\$k)	Travel (\$k)	Total Cost (\$k)
Nominal	\$125	\$30	\$0	\$155
-20%	\$125	\$0	\$0	\$125
-40%	\$93	\$0	\$0	\$93

Table 1: Budget scenarios and money matrix.

**7. Synergies**

**Existing ANL CMOS program:**

We will take advantage of the synergy with the HEP Detector R&D group and the ATLAS pixel group in utilizing the same laboratory, equipment, expertise, and connections. This includes the resources available from the AMS CMOS collaboration for ATLAS ITK Pixels.

**Existing ANL EIC LDRD program:**

An LDRD effort is underway at ANL examining EIC topics in theory, simulation, detectors, and accelerators. This program is exploring the optimization of an EIC detector with 10 ps timing for the tracker and E&M calorimeter to sharpen the design specifications of the detector system. In addition, a silicon detector R&D program focusing on Ultra-Fast Silicon Detectors and timing clock synchronization, both of which compliment the CMOS effort, with the ultimate goal of combining the two technologies.

**Compliment to existing EIC CMOS program at the University of Birmingham:**

The University of Birmingham EIC group is exploring an EIC specific CMOS design for the vertex tracker using CMOS technology from TowerJazz and L-Foundry, whereas we are investigating the AMS technology. As each foundry has unique processing capabilities, it is not known if there will be a clear preference for a specific vendor. Therefore, it is to the advantage of the EIC Detector R&D program to investigate multiple foundry technologies.

## 8. Summary

Early studies indicate that a silicon detector for the electromagnetic calorimeter with timing on the order of 10 ps can handle particle identification at the EIC, while simultaneously reducing the number of subsystems required, reducing the amount of material, and enhancing the photon reconstruction. Combining the gain principles of Ultra-Fast Silicon Detectors with CMOS technology has the potential to provide the ideal silicon detector for an EIC with high granularity pixels and 10 ps timing in a neat monolithic package. We propose to leverage existing CMOS efforts at Argonne in collaboration with the AMS design for ATLAS in order to fully characterize the H35demo and aH18 CMOS samples with an eye towards optimizing features for the EIC. These measurements will include a thorough characterization of the timing properties and comparison to TCAD design. The end result, after one year, will be to prepare an EIC specific design for future fabrication.

## 9. References

- [1] "Electron Ion Collider: The Next QCD Frontier", A. Accardi et al., arXiv: 1212.1701.
- [2] "HVCMOS Sensors for high rate particle tracking", I. Peric, presentation at the 12<sup>th</sup> Trento Workshop, 2017.
- [3] "An overview of CMOS activities for the ATLAS upgrade", E. Vilella, presentation at CLIC Workshop 2017. <https://indico.cern.ch/event/577810/contributions/2477456/>
- [4] "Beam test results of a 16 ps timing system based on ultra-fast silicon detectors", N. Cartiglia, et al., NIM A850, 1 April 2017, pages 83-88.
- [5] "Gain and time resolution of 45 m thin Low Gain Avalanche Detectors before and after irradiation up to  $10^{15}$  n<sub>eq</sub>/cm<sup>2</sup>", J. Lange, et al., arXiv:1703.09004v1, submitted to JINST.
- [6] "Particle pixel detectors in high-voltage CMOS technology—New achievements", I. Peric, C. Kreidl, and P. Fischer, NIM A650, 11 September 2011, pages 158-162.
- [7] "ATLAS Phase-II Upgrade Scoping Document", ATLAS Collaboration, <https://cds.cern.ch/record/2055248?ln=en>.
- [8] <https://geant4.web.cern.ch/geant4/>
- [9] "Prototyping of an HV-CMOS demonstrator for the High Luminosity-LHC upgrade", E. Vilella, et al., JINST 11 C01012, 2016.
- [10] "BeAST Detector (Brookhaven eA Solenoidal Tracker)", A. Kiselev, Presentation at the EIC User Group Meeting, Berkeley, January 2016.