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## EIC Detector R&D Progress Report and Proposal

**Project ID:** eRD25

**Project Name:** Silicon Tracking and Vertexing Consortium

**Period Reported:** January to June 2020

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### Abstract

At the January EIC Detector R&D meeting, eRD16 and eRD18 were invited to form a silicon tracking consortium under the new project identifier eRD25. For the past six months, the two groups have worked closely together to formulate a proposal for R&D toward an EIC-specific Monolithic Active Pixel Sensor at the 65 nm node. This proposal builds upon the prior work of eRD16 and eRD18, and benefits from a collaboration with CERN to develop a sensor for a future upgrade of the inner tracking system of the ALICE experiment. The possibility of higher granularity and lower power consumption offer considerable advantages for an EIC tracking detector in terms of both improved momentum resolution and vertex reconstruction resolution. The performance of the inner tracking system will have a direct impact on several key observables at the EIC, which will be constrained by the performance of the inner tracker. These include the precision measurement of the scattered electron in DIS, the reconstruction of heavy-flavour decays and the measurement of the charged constituents of jets. This proposal presents a design path to an EIC silicon tracking detector starting with the development of the sensor itself.

## 1. Past

### 1.1 *What was planned for this period?*

At the January meeting, eRD16 and eRD18 presented a plan to merge into a unified silicon tracking R&D effort and start working on a concept for the EIC vertex and tracking detector based on the sensor technology proposed for the ALICE ITS3 upgrade. The committee acknowledged and supported the stated plan and encouraged us to present a proposal and funding request for FY21 that would take advantage of this new development.

Following the committee's recommendation, we have used the past six months to analyse more carefully benefits and challenges of the proposed technology and how it could be adapted to the development of an EIC detector. We have also worked toward building a wider collaboration with other groups interested to develop the proposed detector concept.

This section covers the preparations for sensor development, including collaboration building, services R&D, and physics simulations. Building on these, the full proposal for FY21 is detailed in section 2.

### 1.2 *What was achieved?*

#### 1.2.1 *Sensor development*

This effort is based on the close overlap of the ITS3 sensor specifications with the EIC sensor requirements, and the complementary schedules of the two projects. In order to exploit this synergy, discussions with the ALICE ITS3 R&D group have been carried out in the past six months to understand how EIC collaborators can join the development. The ALICE ITS3 R&D group has been clear about their desire for collaboration and have solicited external members to join the R&D design and testing effort. They are currently preparing the framework for integration of external collaborators into the sensor design flow.

The chosen technology for the sensor development is the TowerJazz (TJ) 65 nm imaging process (ISC) and the foundry has recently confirmed support and access to this technology for the duration of the project. Negotiations with TowerJazz are underway to expedite the Non-Disclosure Agreement (NDA) and Process Design Kit (PDK) distribution to collaborators in a coordinated way through CERN, as well as gaining an agreement that the members of the collaboration can share Intellectual Property (IP) blocks. The first stage of this is underway and involving existing members of ALICE and external collaborators that already have an NDA with TJ. This will be extended to all members in a way to be organized at the first "ITS3-WP2: pixel chip design" meeting scheduled for June 25. This meeting will also begin the organization of areas of responsibility based on interest and capability of the collaborators.

The development of the ITS3 sensor is planned around two rounds of Multiple Layer per Reticle (MLR) submissions (no MPW is available in the ISC variant of the TJ 65 nm process), followed by three engineering runs. The two MLR submissions and first engineering run will be carried out together with external collaborators to fully

characterize the technology (charge collection properties, noise, radiation hardness, etc.), develop IP blocks, and gain the necessary design experience. After the first engineering run, it is planned that the external collaborators will fork off their development to design and produce MAPS sensors targeting the specifications of their application.

The first MLR submission (MLR1) is planned for September, and eRD25 is included as one of the participating groups. This has been facilitated by the NDA already available at RAL and by the eRD18 funds that the panel agreed to repurpose to join the ITS3 R&D from the start. This submission will include transistor test structures, simple analogue and digital pixel test structures, IP blocks, etc. We are in the process of defining our contribution and we have been invited to present options for discussion with CERN and other collaborators at the first ITS3 WP2 meeting on June 25. RAL has already installed the required design kit and design work will begin shortly.

In parallel to the discussions with ITS3, we have been in contact with other groups interested in joining the ITS3 R&D effort as a path to an EIC sensor. We have joined together with a group of institutions to form an EIC Silicon Consortium. This currently consists of LBNL, BNL instrumentation division, Birmingham, RAL CMOS Sensor Design group, Wuhan, JLAB, and Daresbury/Liverpool with several other groups expressing strong interest and expected to join soon. The first effort will be concentrated on contributing to the silicon design and characterization, with more of these institutes joining the ITS3 R&D effort formally in the next few months with NDA and access to the PDK.

As the silicon design progresses, we anticipate that the EIC sensor development will fork from the ITS3 development. At this point we will start organizing our own internal work packages to address the parts of the sensor implementation needed for an EIC application. This future work will include mass testing, module design, stave design, disc design, EIC specific infrastructure, etc. It is our intention to develop a full silicon detector implementation and to grow the consortium into an EIC Silicon Detector collaboration.

### *1.2.2 Services parametrisation*

From past experience, the design and performance of the EIC detector will be impacted by the “dead” material in the detector acceptance regions. The EIC detector has a very wide tracking acceptance of approximately  $-4 < \eta < 4$  and a relatively small magnet bore of approximately 2.8 m and is thus relatively “compact”. The effect of the required services and support structures in the limited space require our attention to produce reasonable estimates that can be both used in the detector design to position active silicon and in the full simulation to assess the effect of this material in the detector performance. The intended goal of this parameterization is to be able to produce estimates that are both easy to generate and implement into a GEANT model while also being realistic enough to give reasonable results.

To achieve this, we have put together a parameterized model based on the services of the ITS2 detector staves in ALICE. The characteristics of the services are well known and can be generalized to what could be expected were the EIC detector based on an ALPIDE-like sensor. This model takes both the volume and materials used for reading out ALPIDE in ITS2, averages the material types/volumes to an average radiation length with required volume to contain these services as a function of silicon surface area. This is explained in the presentations in references 1, 2. This approach was then extended to cases including the expected ITS3-like sensor and a reduced services load (for instance using aluminium conductors rather than copper). This allows us to explore the realistic parameter space with regards to the silicon detector layout and performance implications for the full detector.

The services are only one part of the required “dead” material in a detector. As the geometry of a general collider detector is well known and most of the engineered solutions for detector supports are already implemented in the same general way, one can make extrapolations as to what may be expected in the EIC case. The general structure and proposed GEANT-based analogues are described in reference 2. The proposed shapes are again, all simple geometric shapes that should lend themselves well to implementation in the simulations.

The overall goal of these parameterizations is to explore the implications that these estimates have on detector performance and to then be able to identify areas where targeted R&D may be necessary to address performance issues based on the results.

### *1.2.3 Physics simulations*

The simulation efforts of both eRD16 and eRD18 have until recently been performed mainly in the EICroot simulation framework developed by the BNL task force. Single-track resolution studies have been performed for conceptual layouts using different numbers of and positions for the barrel layers and forward/backward disks in both all-silicon and hybrid tracking configurations, and the effects of different pixel sizes (point resolution) had been evaluated. When these efforts started, eRD16 focused mostly on the disks and eRD18 targeted the barrel region; more recently the groups have worked together towards integrated designs.

At the January 2020 EIC generic detector R&D meeting, the “EIC Yellow Report” effort had just started and it became increasingly clear that EICroot development would cease. Following the January meeting, we have thus made a start on transitioning towards the supported frameworks ESCalate (G4E+eJANA) and Fun4All. New simulations have been performed with EICroot as well [3], for example to make a start on investigating the impacts of the increased diameter of the beampipe (62mm) in the eRHIC design compared to the diameter that had been assumed for the original BeAST detector concept (36mm) and in most of the prior eRD16 and eRD18 simulations.

H. Wennl f did most of the work on ESCalate and has reported benchmark comparisons with earlier eRD18 simulations in an EIC Yellow Report tracking working group meeting in May 2020 [4]. At that time, the single-track performance for similar

GEANT geometries showed that ESCalate produced the same general trends as a function of momentum and pseudo-rapidity to those found in EICroot but that were consistently worse than those results. The ESCalate results were based on G4e and GenFit tracking. The implementation of ACTS tracking is being worked on by the main ESCalate developers but this is not yet finished. Consequently, a decision has been made to redirect further simulation effort at Birmingham towards Fun4All.

Benchmark studies are currently being performed against previously simulated detector configurations in EICroot [5]. The same configuration can be simulated in the two frameworks by exporting the EICroot GDML geometry and importing it into Fun4All. Material scans have confirmed that the EICroot configurations can be imported correctly into Fun4All. Figure 1 shows a comparison of the relative momentum resolution as a function of momentum for an all-silicon detector configuration previously simulated by eRD18 in EICroot. Good agreement is observed between the results obtained in the two frameworks, giving confidence in their validity. Further benchmark studies are ongoing to compare results on impact parameter resolution. In parallel, Pythia studies have been made to investigate and quantify the theoretical impact of pixel size on charmed meson ( $D_0$ ) decay vertex separation. This study will be repeated using Pythia event propagation through the simulation.

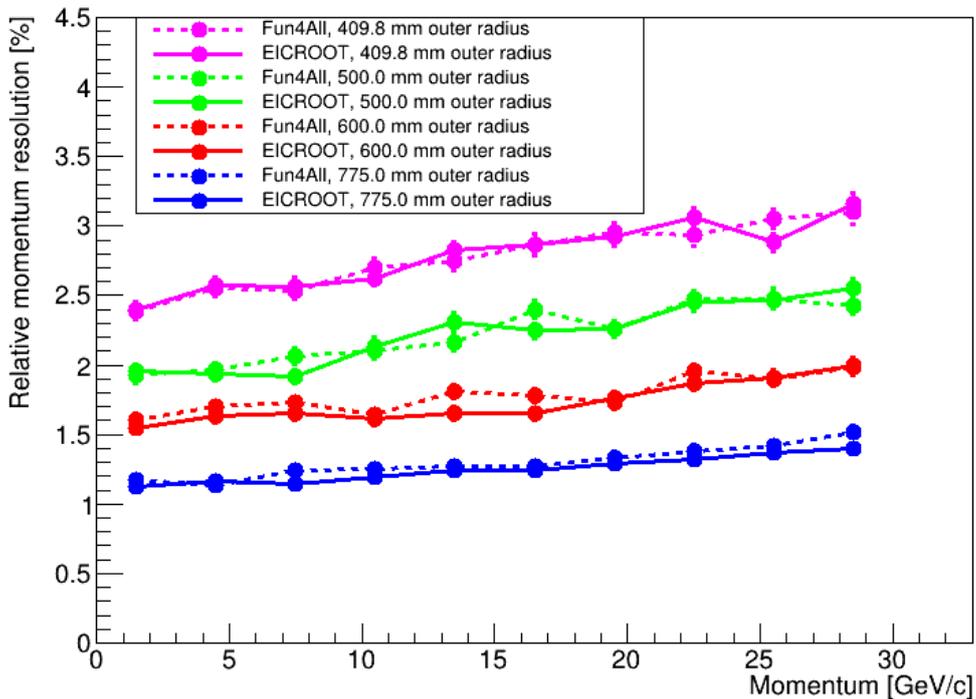


Figure 1. Comparison of the relative momentum resolution as a function of momentum for an all-silicon geometry simulated in EICroot and Fun4All. The simulation covers cases of different outer radii for the detector.

Concurrently, R. Cruz-Torres led LBNL/UCB efforts to transition from EICroot to Fun4All and to use this framework on the NERSC Cori compute facility so that more granular studies could be performed of the pseudo-rapidity and other single-track dependences. In these studies, the GEANT geometry was exported from EICroot and

imported into Fun4All. Single-track performance was found to be in satisfactory agreement with prior EICroot results obtained by Y.S. Lai et al. More detailed studies and scans have been performed, for example of material budget including a cone-like structure to mimic the effects of services and supports based on initial estimates described in section 1.2.2. This is illustrated in Figure 2, which shows results from a material scan versus  $\eta$  [6].

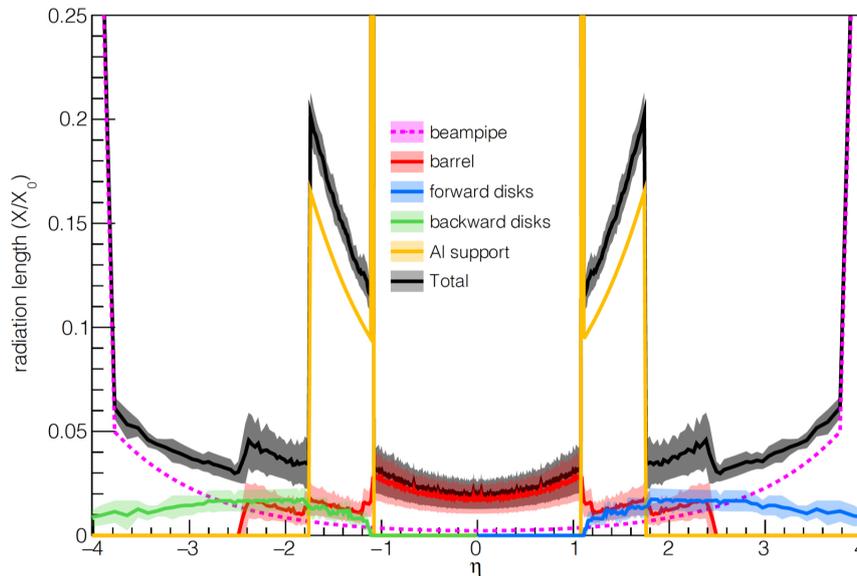


Figure 2. Material scan versus pseudo-rapidity for the eRD16 all-silicon detector concept. This concept includes an initial implementation of parametrized services and supports, in addition to a detailed description of the actual stages. The support and services are guided out in a projective way near  $\eta = -1$  and  $\eta = 1$ , as reflected by the large increase in radiation length at these  $\eta$ . The increased level in the region  $1.0 < |\eta| < 1.8$  has its origins in the cylindrical support and services surrounding the outer radii of the forward and backward disks in this concept; they do not affect tracking performance. The remaining structures reflect acceptance transitions as indicated.

Fun4All simulations of the eRD16 all-silicon concept have been used also to quantify the angular resolutions at the PID subsystems, which turn out to impose stringent requirements on the tracking subsystems [7]. Representative results are shown in Figure 3, where the polar angular resolution is calculated at the outermost tracking layer.

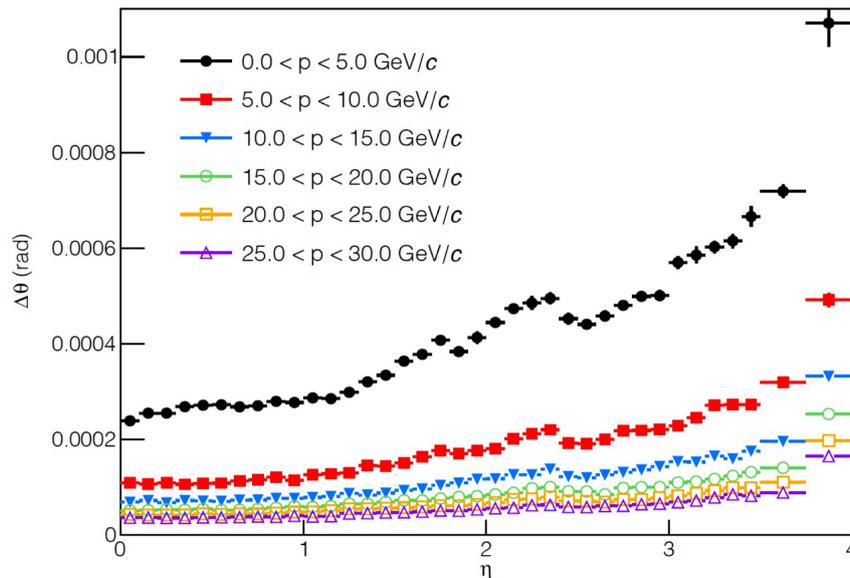


Figure 3. Polar angular resolution versus pseudo-rapidity for the eRD16 all-silicon detector concept.

As this report is being written, the GEANT-based Fun4All response simulations have been successfully interfaced with the Pythia 8 event generator and initial simulations of jet reconstruction capabilities have been performed.

The transition to a simulation framework that will be supported in the longer term within and for the EIC community is thus well advanced though not yet complete. It currently focuses on Fun4All. A subset of existing EICroot simulations have been repeated with Fun4All and new studies that go beyond prior EICroot work have been performed. Services and supports are part of several of the Fun4All simulations, albeit thus far still mostly with a geometry that was imported from EICroot.

### 1.3 What was not achieved, why not, and what will be done to correct this?

The ITS3 schedule and work on sensor development have been affected by delays due to longer than anticipated discussions with TJ to confirm support and access to the 65 nm ISC process. As such, work on the 65 nm process that was due to start in February, is only just starting.

As explained in section 1.2.1, TJ has now agreed to support the process and made MLR available to the collaboration. The first MLR submission (MLR1) is planned for September, and a new ITS3 schedule has been approved by the LHCC. The new schedule is still compatible with the EIC timeline towards a TDR.

Meetings of the “ITS3-WP2: pixel chip design” start on June 25 and a set of written understandings is in preparation that collaborators will need to follow to join the R&D programme. CERN is working on facilitating access to the technology via NDA, with RAL already included in the MLR1 design effort given their previously existing NDA with the foundry, Berkeley and other EIC Silicon Consortium institutes to be added in the next few months.

*1.4 How did the COVID-19 pandemic and related closing of labs and facilities affect progress of your project?*

The work planned for this period was not affected by the closing of labs as it did not have a component that required access to lab facilities for use of equipment.

*1.5 How much of your FY20 funding could not be spent due to pandemic related closing of facilities?*

Berkeley: Not applicable (note, however, that FY20 eRD16 funds are remaining as this report is being prepared for reasons that are not specifically related to the COVID-19 pandemic).

Birmingham: approximately half of the travel budget from FY20 is unspent.

*1.6 Do you have running costs that are needed even if R&D efforts have paused?*

No.

## 2. Future

*2.1 What is planned for the next funding cycle and beyond? How, if at all, is this planning different from the original plan?*

The EIC vertex and tracking detector will form the innermost part of a future EIC experiment. It has to fulfil three tasks: determine primary vertices with high precision; allow the measurement of secondary vertices for heavy-flavour decays; and track low- $p_T$  particles. High granularity and low material budget are needed to perform these measurements to the required accuracy. Simulations quantify the required spatial resolution to be around 5  $\mu\text{m}$ , and a material budget in the region of 0.1-0.2%  $X_0$  per layer. An interaction frequency in the range 50 – 500 kHz translates into an integration time of 2  $\mu\text{s}$ . These constraints are summarised in the Electron-Ion Collider Detector Requirements and R&D Handbook [8].

Previous work carried out by eRD16 and eRD18, informed a technology survey presented at the first Yellow Report Workshop [9]. The detector technology identified to meet the requirements specified above is Monolithic Active Pixel Sensors (MAPS). However, none of the existing MAPS detectors is designed to fulfil all of these requirements at once, so that a dedicated sensor development is needed for the EIC vertex and tracking detector.

Work from eRD18 has shown that a sensor suitable for the EIC could be produced at the 180 nm node. However, by the time the EIC begins operation (2029-30) this node could be obsolete. It is therefore not only desirable but also sensible to explore more advanced process nodes to guard against obsolescence and to ensure the highest performance of the EIC detector. The most attractive option is the 65 nm node, as this represents a step change in technical performance and has received a lot of interest from the particle physics community. With respect to previous technology nodes, the 65 nm node offers the improved low power and high granularity features that are key for high precision measurements at the EIC. The downside is that it has an increased cost compared to the 180 nm process.

However, an opportunity has arisen to access this advanced process at reduced cost by working with other institutions. The ITS3 upgrade for ALICE plans to use the TowerJazz 65nm process, and we have the opportunity to become involved in this design effort and use the results in EIC applications. This offers significant potential advantages to the EIC. For example, it will allow cheaper access to this advanced process thanks to shared silicon costs. Furthermore, the design risk and effort required will be reduced, since we will build on planned developments for ALICE to develop an EIC tracking and vertex detector.

To realise these benefits, it is crucial to take advantage of this opportunity now. Whilst the ALICE development is similar to the requirements and timescale of the EIC, it is not identical. At some stage we will need to “fork” the design and develop an EIC specific device. The earlier we get involved, the easier this will be. From a practical standpoint, collaborations to work at the 65 nm node are forming now. If we are not involved at an early stage, our influence on the direction of the design will be reduced, and it may not be possible to get involved at a later stage. In FY21, we are requesting R&D funds to start working with the CERN team on test structures at the 65 nm node. This will allow us to gain experience with the 65 nm process and establish the viability of this approach to developing an EIC detector. If this approach proves successful, having made this initial investment will put us in an excellent position to exploit similarities between ITS3 and EIC requirements, improving performance and reducing development costs.

In parallel to the sensor development activity, in FY21 we will work on the definition of a detector concept based on the proposed sensor technology. Physics performance simulations will be carried out to optimise the detector configuration and will include a realistic description of the detector services with the goal of identifying areas that need targeted R&D to achieve the required material budget.

The ITS3 project is taking an integrated approach where design and post-processing techniques are combined to develop a three-layer vertex detector with high granularity (10  $\mu\text{m}$  pixel pitch) and a material budget of 0.05%  $X_0$  per layer. The use of low power, large area, 2D stitched sensors thinned below 50  $\mu\text{m}$  and bent around the beam pipe minimises cooling, support structure and services in active area. Such a detector concept is certainly attractive for the EIC vertex layers. Preliminary EICRoot simulations have indicated a significant gain in vertexing capabilities, beneficial in particular after the recent increase of beam pipe radius. Figure 4 compares the transverse impact parameter resolution versus momentum for a hybrid tracking configuration (silicon MAPS and a TPC) in three cases: baseline detector geometry for the old beam pipe design (green); baseline detector geometry for the new, larger-radius beam pipe (blue); and baseline detector geometry for the larger-radius beam pipe with ITS3 detector parameters for the vertex layers. The simulation studies pions in a momentum range up to 5 GeV/c in the pseudorapidity range  $-0.5 < \eta < 0.5$ . A uniform 1.5T magnetic field is assumed. For the curves labelled “ITS2”, the detector parameters are: 20  $\mu\text{m}$  pixel pitch, 0.3%  $X_0$  for the inner layers and 0.8%  $X_0$  for the outer layers. The curve labelled ITS3 has 10  $\mu\text{m}$  pixel pitch is used, with 0.05%  $X_0$  in

the vertex layers. The outer layers are kept at  $0.8\% X_0$ . These results show that without an aggressive development for the innermost vertex layers, detector performance would be significantly affected by the increased beam pipe radius.

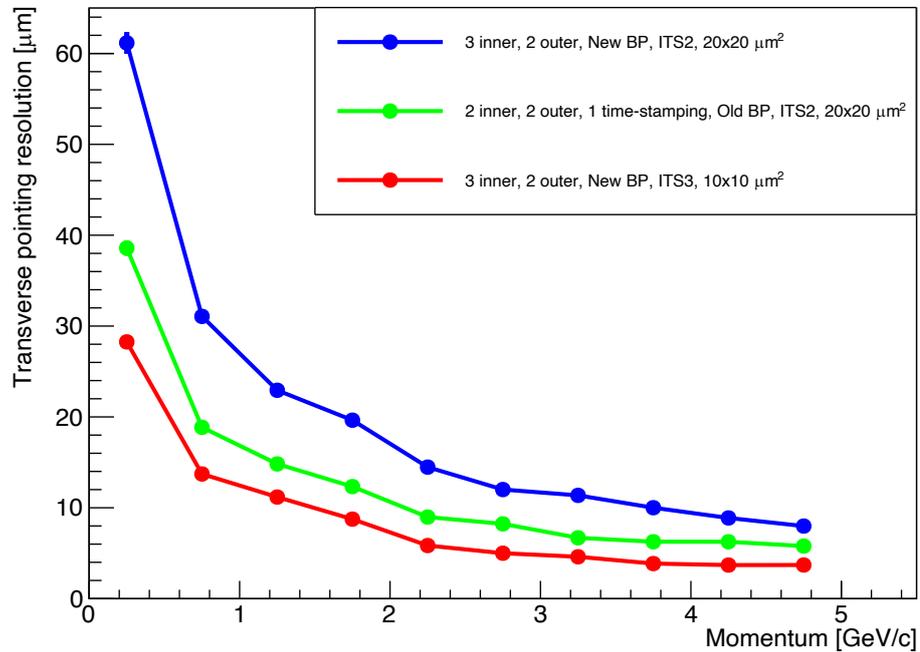


Figure 4. Transverse impact parameter resolution versus moment for a hybrid tracking configuration in three cases: baseline detector geometry for the old beam pipe design; baseline detector geometry for the new beam pipe design; and baseline detector geometry for the new beam pipe design with ITS3 detector parameters.

Likewise, we have identified advantages from the further reduced material (below the required  $0.1\text{-}0.2\% X_0$ ) in the forward/backward disks and note that the increase in beam pipe radius will reduce the acceptance of the innermost barrel layers underlining the need to revisit the integration with the forward disks from a vertexing standpoint.

Although the yield of the newly proposed larger-than-reticle size ITS3 sensors is not currently known, we anticipate that yield may very well preclude the use of the ITS3 extremely low mass approach throughout the entire silicon tracking subsystem. Regions of highest benefit thus will need to be identified, which is likely to hold also from the perspective of future cost-optimization. In regions where the use of this mass-optimized approach is not necessary or not practical, we anticipate using the more conventional configuration of staves and disk supports and achieving material reduction with dedicated engineering solutions.

In summary, our proposal for FY21 aims at

- Joining the emerging ALICE ITS3 R&D program on 65 nm technology to gain the required expertise to design a (ITS3-derived) MAPS sensor for the EIC;
- Developing and investigating the performance of well-integrated and large-acceptance tracking concepts with barrel layers and forward/backward disks;
- Identifying areas requiring targeted services R&D.

The following sections, 2.1.1 and 2.1.2, detail how this work will be carried out.

### *2.1.1 Sensor development*

The work on sensor development in FY21 will start with the characterisation of the test structures submitted in the MLR1 described in section 1.2.1. Characterisation will be carried out at LBNL and Birmingham, with emphasis on charge collection properties of the pixel analogue test structures and testing of the IP blocks we proposed. For a complete characterisation we plan to carry out tests in clean rooms with radioactive sources and TCT measurements. The irradiation facilities at the MC40 Cyclotron in Birmingham and at the 88-Inch Cyclotron in Berkeley will be used to characterise the structures with respect to bulk damage, TID effects, and Single Event Effects. This work will be part of an extensive characterisation programme.

Following this we plan to contribute to the second ITS3 MLR submission, currently planned for September 2021. The goal for this is to build on the test structures and small IP blocks submitted in the MLR1 and develop more complete readout architectures and pixel matrices, moving one step closer to a full chip. We are requesting funding for designer time at RAL to support this process and to contribute to MLR2 costs.

We anticipate that more EIC Silicon Consortium institutes will join these activities, providing characterisation effort and contributing test structures to the MLR2. In this manner we aim to achieve the goal laid out in previous sections of having sufficient knowledge and involvement in the ITS3 design to be able to develop it into an EIC specific sensor at minimum risk in the future.

### *2.1.2 Physics simulations*

A number of simulation efforts related to charged-particle tracking at EIC using subsystems based on silicon-sensors are ongoing. An important recent development is the change (increase) in the diameter of the beampipe of the eRHIC design compared to the assumptions carried over from the earlier BeAST detector concept. The crossing angle of the beams, which is now known as well, has further implications for the overall inner tracking system. Both aspects, as well as ITS3 related sensor development, will require further simulation effort.

For the upcoming funding cycle, we propose to focus our (eRD25) simulation effort on further developing and investigating the performance of well-integrated and large-acceptance tracking concepts with barrel layers and forward/backward disks. Both all-silicon and hybrids including silicon tracking subsystems will be considered. New elements include the possibility to incorporate curved wafer-scale and ultra-thin silicon sensors afforded by the ITS3-derived sensor development. We anticipate that these will have a place in specific acceptance regions at the EIC, but that the layers and disks furthest from the interaction region will use more conventional geometries for reasons of sensor yield and cost considerations. An important goal is thus to investigate where these potential advantages will offer the largest benefits to EIC

tracking and vertexing performance and where the more conventional stove-based approaches are appropriate. The newly proposed effort will build on the now largely integrated eRD16 and eRD18 simulation work in Fun4All and will extend this work to incorporate realistically modelled services and supports based on the work discussed in section 1.2.2 with the further goal to identify areas for EIC-specific targeted R&D.

Specifically, we propose to determine single-track performance that factors in both the demands from physics measurements and the developing demands that surrounding sub-systems impose on the tracking. An example of the latter are the angular pointing resolutions at the particle-identification sub-systems, which as an intermediate outcome of the “EIC Yellow Report” effort, are now known to be particularly stringent. We furthermore propose to simulate the measurement capability for deep-inelastic production of open-charm, a process that combines the need to precisely measure the scattered electron over a broad acceptance with the need to determine the displaced decay vertex of the charmed hadrons. These physics simulations will also give insight in the hit densities from beam collisions. (While detailed understanding of hit densities from backgrounds is needed as further input for our proposed sensor development, we note that the eRD21 project focuses on background studies).

We note that a number of other studies, for example for the ongoing “EIC Yellow Report” effort, make use of parametrized single-track performance and physics event-generators to make projections of future measurement capability (fast-simulations). While the single-track response is in several cases based on or derived from eRD16 and eRD18 simulations and it seems probable to us that this will hold also for future eRD25 simulation results, we consider fast-simulations outside the scope of the eRD25 project.

### *2.1.3 What are critical issues?*

One potential critical issue is the access to laboratory and irradiation facilities over part of the period necessary for characterization of the MLR1 test structures due to social distancing regulations or new lockdown measures. This could hinder development of the next submission as feedback on the technology would be delayed. Whilst the likelihood of this issue and its impact are difficult to assess at the moment, the fact that a large collaboration of institutes in different countries will be working on the characterization might in part mitigate the risk.

### *2.1.4 Additional information*

No additional information.

## **3. Request for resources**

Wherever possible existing resources will be devoted to the project. This includes personnel time, computing resources and consumables (see Personnel and External funding). Design effort towards the implementation of test structures for the first ITS3 65 nm MLR submission in September 2020 will be paid with remaining eRD18 funding.

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Work on simulations and characterization of test structures will be carried out with post-docs and PhD students at LBNL/UCB and Birmingham.

We request funds to continue engagement with ITS3 and work on the 65 nm process. This includes chip designer time at RAL to work on test structures for the ITS3 MLR2, and money to contribute to the MLR2 submission. Funding is also requested to purchase readout systems for characterisation of the MLR1 test structures, and development of carrier boards for dedicated studies of our IP blocks. No request is made for travel as restrictions might continue for the duration of the project.

Optimal budget scenario:

- 6 months of designer time to develop 2-3 complex IP blocks, or perhaps a matrix of test pixels with a simple readout;
- Purchase of the readout system from the collaboration and fabrication of daughter boards to test our test structures;
- Personnel for the development of hardware, firmware, software needed for full characterization of our IP blocks and analogue pixel test structures submitted by the collaboration.

| k\$               | Chip design | Silicon submission | Consumables | Engineer | Total      |
|-------------------|-------------|--------------------|-------------|----------|------------|
| <b>RAL</b>        | 115         | 40                 |             |          | 155        |
| <b>LBNL</b>       |             |                    | 18          | 16       | 34         |
| <b>Birmingham</b> |             |                    | 12          | 12       | 24         |
| <b>TOTAL</b>      |             |                    |             |          | <b>213</b> |

Intermediate budget scenario:

- 4 months of designer time to develop 1 complex IP block;
- Purchase of the readout system from the collaboration and fabrication of daughter boards to test our test structures;
- Personnel for the development of hardware, firmware, software needed for full characterization of our IP blocks only.

| k\$               | Chip design | Silicon submission | Consumables | Engineer | Total      |
|-------------------|-------------|--------------------|-------------|----------|------------|
| <b>RAL</b>        | 70          | 40                 |             |          | 110        |
| <b>LBNL</b>       |             |                    | 18          | 8        | 26         |
| <b>Birmingham</b> |             |                    | 12          | 6        | 18         |
| <b>TOTAL</b>      |             |                    |             |          | <b>154</b> |

Minimal budget scenario:

- 4 months of designer time to develop 1 complex IP block, but lower contribution to shared run costs may lead to less area/influence;
- Purchase of the readout system from the collaboration and fabrication of daughter boards to test our test structures;
- Personnel for the development of hardware, firmware, software needed for full characterization of our IP blocks only.

| k\$               | Chip design | Silicon submission | Consumables | Engineer | Total      |
|-------------------|-------------|--------------------|-------------|----------|------------|
| <b>RAL</b>        | 70          | 25                 |             |          | 95         |
| <b>LBNL</b>       |             |                    | 18          | 8        | 26         |
| <b>Birmingham</b> |             |                    | 12          | 6        | 18         |
| <b>TOTAL</b>      |             |                    |             |          | <b>139</b> |

#### 4. Personnel

##### Lawrence Berkeley National Laboratory

The simulation efforts during this reporting period were carried out part-time by postdoctoral researcher R. Cruz-Torres, Project Scientist Y.S. Lai and E.S. Lai's EIC effort has in parts been supported by eRD16 funds and concerns simulations within the BNL-developed EICroot framework. Lai is stationed at LBNL and supervised by B.V. Jacak. The sensor and services efforts during this reporting period were carried out part-time by L. Greiner.

##### University of Birmingham

Prof. P. Jones and Dr. L. Gonella spend approximately a fraction of 0.1 and 0.2 FTE respectively on the project at no cost. They supervise two PhD students, H. Wennlöf and S. Maple, who work full time on the project, fully funded by the School of Physics and Astronomy of the University of Birmingham. Dr. P. Ilten has joined the supervision of H. Wennlöf providing support for Pythia and guidance for physics simulations. Prof. P. Allport and Prof. P. Newman have an advisory role and participate in our regular project meetings to monitor progress.

##### RAL CMOS Sensor Design group

I. Sedgwick (or other chip designer) works on the project according to the awarded funding. Previous funding awarded for eRD18 has covered in total 6 months of chip designer time. N. Guerrini has an advisory role and participates in our regular project meetings to monitor progress.

#### 5. External funding

##### Lawrence Berkeley National Laboratory

Several LBNL staff members and colleagues from other University of California (UC) campuses are part of a successful pilot project as the outcome from our response to a 2019 UC Multi-campus Research Funding Opportunity (MRPI). Although the work reported here was not funded directly through this UC proposal and Laboratory staff cannot be supported through this opportunity, closely related work has been performed in the context of the "EIC Yellow Report" with MRPI funds. Our follow-on Letter-of-Intent in response to a new 2021 MRPI has been accepted to proceed to a full proposal. This proposal will be submitted in Summer; its outcome is obviously not currently known.

B.V. Jacak was named a 2019 Distinguished Scientist Fellow by the U.S. Department of Energy. This award has made it possible to attract postdoctoral researcher R. Cruz-Torres, who has performed a number of simulations contained in this work. This award has funded also undergraduate students who have performed closely related simulations.

A. Collu and several other LBNL staff members have submitted a 2021 LDRD proposal aiming to pursue and address several key issues related to the development, interconnection and powering of larger than reticle size and up to wafer-scale sensors in the TowerJazz 65nm CMOS process for EIC purposes. This proposed effort is distinct from the effort proposed here and the proposal outcome is not currently known.

#### University of Birmingham

The University of Birmingham provides funds to support two 3.5-year Ph.D. studentship: one was taken up by H. Wennl f in September 2017, and one has just been awarded to S. Maple to start in September 2020.

In addition, our bid to support some of the R&D elements of this proposal through EU Horizon 2020 has been successful. This formed part of the NextDIS work package included in the STRONG-2020 proposal. The proposal has been awarded €62.5k to support the submission of an EIC DMAPS sensor prototype.

A UK EIC-project, proposed by us, has been invited to participate as a Preliminary Activity to the UKRI Infrastructure Fund. The proposal, submitted by a collaboration of UK institutes from nuclear and particle physics (PI: P. Jones, Birmingham, and D. Sokhan, Glasgow), is structured around detector R&D for vertex and tracking, polarimetry, and far-forward detectors. Funding has been requested for three years, starting in 2021-22. The Universities of Birmingham, Liverpool and Lancaster, and STFC Daresbury, RAL PPD and RAL CMOS Sensor Design group have requested approximately £2.7M to develop an R&D programme to design an EIC-specific MAPS sensor in 65 nm technology, readout systems, cooling and mechanical design.

## **6. Publications**

None at this stage of the project.

## **7. References**

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2. L. Greiner, Si material projections, <https://indico.bnl.gov/event/8231/contributions/37955/>, 2<sup>nd</sup> EIC Yellow Report Workshop, 21 May 2020
3. H. Wennl f, Status of tracking simulation studies in the EICRoot, <https://indico.bnl.gov/event/7894/contributions/37624/>, EIC-YR Tracking WG weekly meeting, 14 May 2020

4. H. Wennl f, Status of tracking simulation studies in the ESCalate framework, <https://indico.bnl.gov/event/7893/contributions/37285/>, EIC-YR Tracking WG weekly meeting, 7 May 2020
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7. R. Cruz-Torres, Update on All-Silicon Tracker Implementation in Fun4All, <https://indico.bnl.gov/event/7894/contributions/37609/>, EIC-YR Tracking WG weekly meeting, 14 May 2020
8. Electron-Ion Collider Detector Requirements and R&D Handbook, [http://www.eicug.org/web/sites/default/files/EIC\\_HANDBOOK\\_v1.2.pdf](http://www.eicug.org/web/sites/default/files/EIC_HANDBOOK_v1.2.pdf)
9. L. Gonella, Survey of Silicon Detector Technologies, <https://indico.bnl.gov/event/7449/contributions/35954/>, 1<sup>st</sup> EIC Yellow Report Workshop, 19 March 2020