



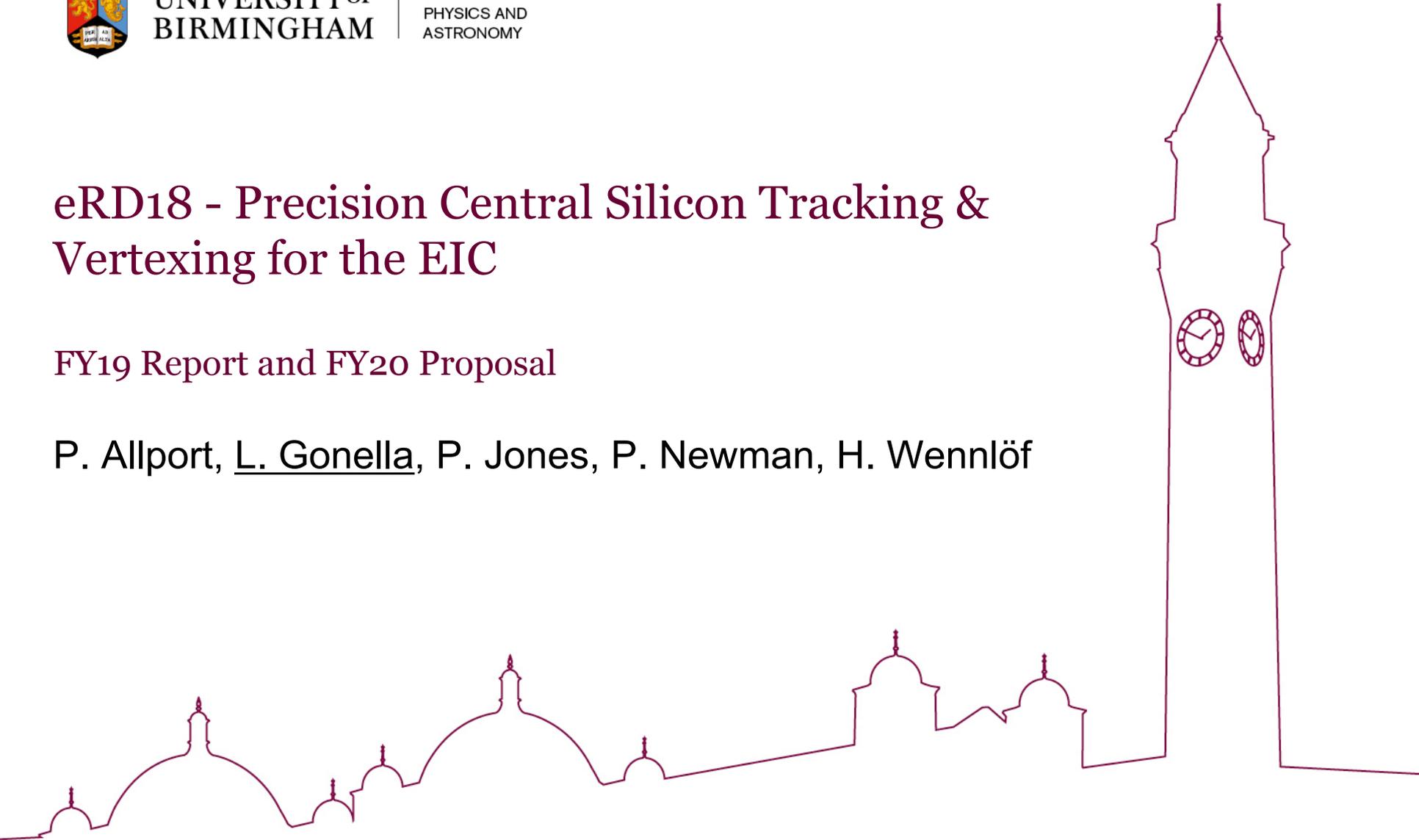
UNIVERSITY OF  
BIRMINGHAM

SCHOOL OF  
PHYSICS AND  
ASTRONOMY

# eRD18 - Precision Central Silicon Tracking & Vertexing for the EIC

FY19 Report and FY20 Proposal

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# Proposal

To develop a detailed concept for a central silicon vertex detector for a future EIC experiment, exploring the potential advantages of depleted MAPS (DMAPS) technologies

## Science drivers

Open heavy flavour decays – **high position resolution**  
Precision tracking of high  $Q^2$  scattered electrons – **low mass**

## WP1: Sensor Development

Exploit on-going R&D in Birmingham into depleted MAPS to investigate potential solutions for the EIC

## WP2: Silicon Detector Layout Investigations

Performance requirements: numbers of layers, layout and spatial resolution of the pixel hits

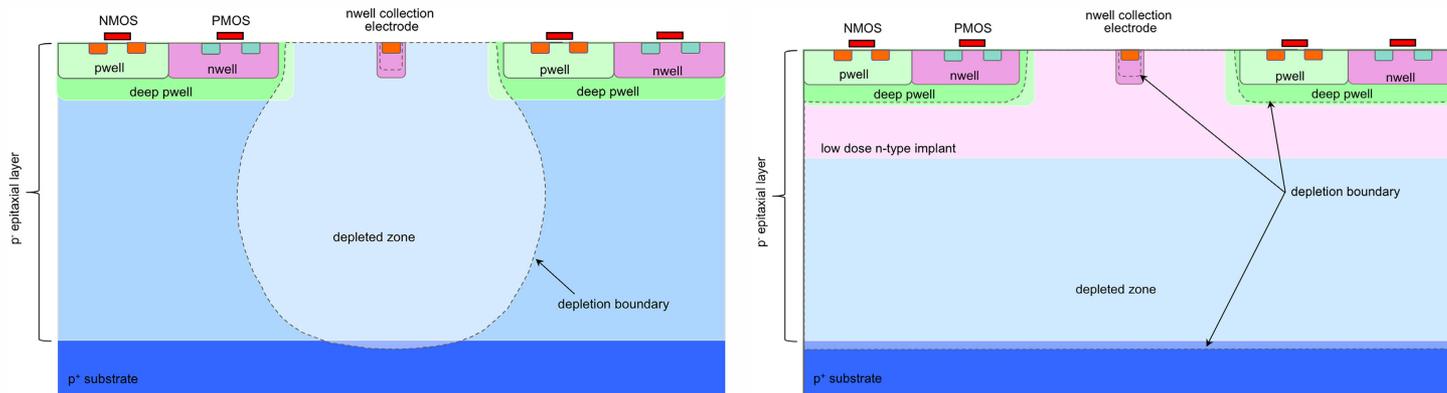


# WP1: Sensor development

- Towards an EIC-specific DMAPS sensor
  - Aim for improved spatial resolution with respect to ALPIDE
    - Smaller pixels ( $20 \times 20 \mu\text{m}^2$ )
    - Low mass detector layers ( $< 0.3\% X/X_0$  - low power)
  - Consider readout requirements for the EIC
    - Integration time and time-stamping capability
- Previous work
  - Technology identified: TowerJazz modified process
  - Defined preliminary specifications for EIC-specific DMAPS sensor
- Work planned for FY19
  - **Technology investigation**
    - Complete comparison of TJ investigator chips
  - EIC specific DMAPS **design study** in collaboration with RAL CMOS sensor design group

# WP1: TJ 180nm CMOS imaging technology

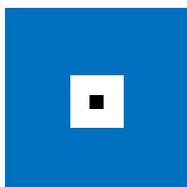
- Standard process
  - Used by the ALICE ITS ALPIDE sensor
  - Small collection electrode = low detector capacitance
  - Partially depleted; charge collection in part by drift
- Modified process
  - Developed by CERN-TJ collaboration for HL-LHC tracker upgrades
  - Deep planar junction allows full depletion with small collection electrode
  - Enables small pixels, low noise, and low power



W. Snoeys et al, <http://dx.doi.org/10.1016/j.nima.2017.07.046>

# WP1: TJ Investigator Chips

- TJ investigator chips provide test structures to study charge collection properties of different pixel layouts in the modified process
  - Tests carried out in the lab with  $^{55}\text{Fe}$
- Each chip has 134 matrices of 10 x 10 pixels
  - Variables are pixel pitch, electrode size and electrode spacing



Pixel:  $28 \times 28 \mu\text{m}^2$   
Electrode:  $2 \times 2 \mu\text{m}^2$   
Electrode spacing:  $3 \mu\text{m}$

## Available pixel matrices

0-35:	$20 \times 20 \mu\text{m}^2$
36-57:	$22 \times 22 \mu\text{m}^2$
58-67:	$25 \times 25 \mu\text{m}^2$
68-103:	$28 \times 28 \mu\text{m}^2$
104-111:	$30 \times 30 \mu\text{m}^2$
112-123:	$40 \times 40 \mu\text{m}^2$
124-133:	$50 \times 50 \mu\text{m}^2$

## Electrode sizes

$1-5 \mu\text{m}^2$

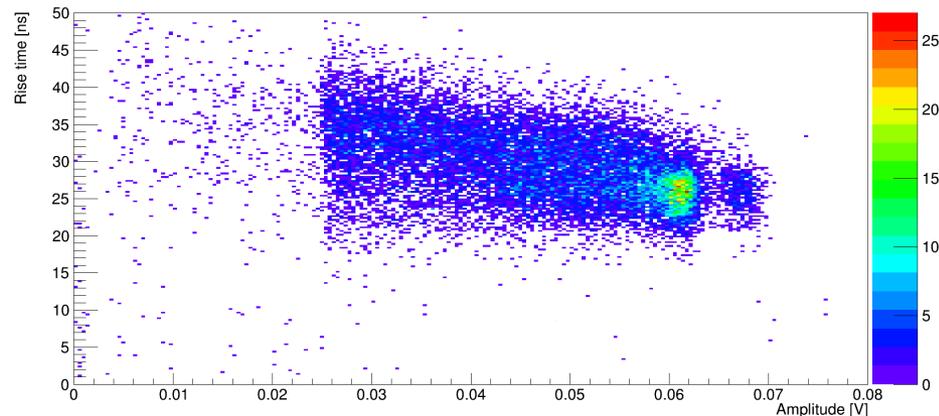
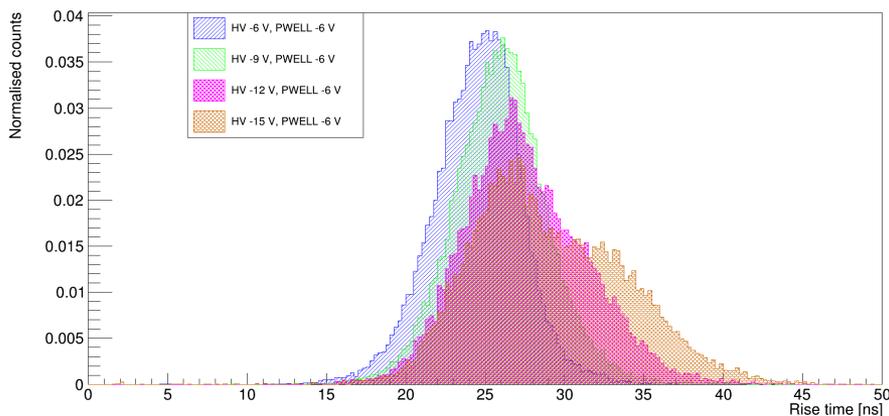
## Electrode spacing

$1-5 \mu\text{m}$  typically  
(except matrix 112-133 in TJ1 and TJ1b)

- Three different versions available: TJ1, TJ1b, TJ2
- Improved charge collection in TJ1b and TJ2
  - Separate bias for p-substrate and the p-well (TJ1b and TJ2)
  - Reduced electrode spacing for large pixels (TJ2)
  - Faster readout capability (TJ2)

# WP1: Rise time test with TJ1b

- Tests focus on TJ1b to investigate effect of increased bias
  - $^{55}\text{Fe}$  source test on  $28 \times 28 \mu\text{m}^2$  pixel
- By increasing the bias voltage, the rise time increases and the distribution widens, tending towards a bimodal distribution
  - The pulses with higher rise time are correlated to the hits with smaller amplitude, possibly from charge sharing at the edge of the pixel



## ■ Comments

- This behaviour is not observed in smaller pixels (i.e.  $20 \times 20 \mu\text{m}^2$  pixel)
- ATLAS MALTA DMAPS sensor measured low efficiency from pixel edges (R. Cardella et al, 2019 JINST 14 C06019)

## WP1: Sensor design and charge collection properties

- TCAD simulations carried out by colleagues at CERN shown that charges from the edge of the pixel drift along longer paths
  - M. Munker et al, 2019 JINST 14 C05013
  - Charges are first pushed towards a potential minimum between pixels and then drift laterally towards the collection electrode
  - Increasing the HV leads to even slower charge collection and reduced signal from the edges of the pixel

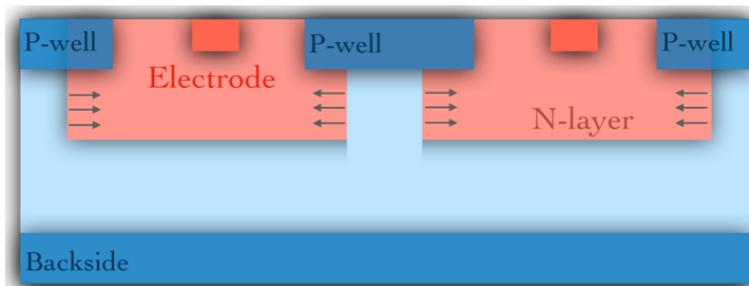
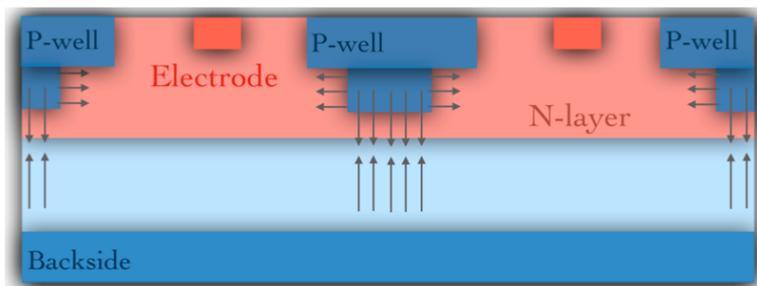
TCAD simulation - electrostatic potential minimum at pixel border:



- Our findings are consistent with these simulations

## WP1: Improvements to sensor design

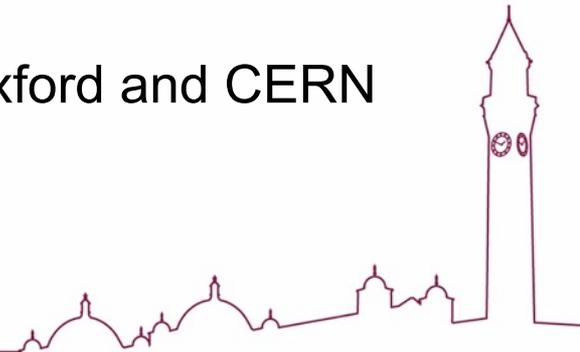
- The critical design parameter is the extent of the p-well
  - For pixel size larger than  $20 \times 20 \mu\text{m}^2$
- Two technology modifications have been simulated in TCAD showing potential for more uniform charge collection in the pixel
  - Gap in the deep n-well between pixels or extra deep p-well between pixels
- Electric field lines bend towards the collection electrode
  - More uniform signal expected over the pixel
  - Charge collection improved by increased HV



M. Munker, <https://indico.cern.ch/event/669866/contributions/3234996/>

# WP1: Test beam results on Mini-MALTA

- These modifications have been implemented in the Mini-MALTA
  - ATLAS DMAPS sensor based on MALTA design
    - 36.4 x 36.4  $\mu\text{m}^2$  pixel, 3-4  $\mu\text{m}$  spacing, 25 ns integration time
    - Column drain readout architecture design for HL-LHC
  - Different sectors implementing the three sensor design variants for comparison
- We are working on test beam data analysis of the Mini-MALTA
  - Beam test at the Diamond facility
  - Focused 8 keV X-ray beam scanned in 2  $\mu\text{m}$  steps over the sectors
  - Preliminary results indicate uniform charge collection in the pixel
- Results are being prepared for publication with Oxford and CERN colleagues and will be presented in January



# WP1: Summary of technology investigations

- The TJ modified process improves charge collection properties but the sensor layout is crucial
  - Increasing the substrate bias voltage can be beneficial for charge collection properties in conjunction with the n-gap or extra deep p-well modifications
- As the TJ investigator chips are no longer representative of the latest process implementation, technology characterisation will continue with more recent prototypes
  - A summary of the results obtained on all three TJ investigator chips has been compiled and submitted to the committee
  - The Mini-MALTA results will be published soon
- For an EIC DMAPS sensor of 20  $\mu\text{m}$  pixel pitch
  - The modified process achieves significant improvement cf. ALPIDE
  - The extra modifications can potentially be beneficial
  - Increased HV capability is not required

# WP1: EIC DMAPS sensor specifications

- Two sets of specifications
  - Primary objective: vertex and tracking detector
  - In addition: investigate feasibility of time-stamping layer
- Specifications updated together with chip designer at RAL
  - Power, noise and fake hit rate based on ALPIDE specifications
  - Max pixel size for a time stamping layer calculated to match the TPC resolution

	EIC DMAPS Sensor	
Detector	Vertex and Tracking	Timing Layer
Technology	TJ or similar	
Substrate Resistivity [kohm cm]	1	
Collection Electrode	small	
Detector Capacitance [ff]	<5	
Chip size [cm x cm]	Full reticule	
Pixel size [ $\mu\text{m} \times \mu\text{m}$ ]	20 x 20	max 350 x 350
Integration Time [ns]	2000	2000
Timing Resolution [ns]	N/A	< 9 (eRHIC) < 1 (JLEIC)
Particle Rate [kHz/mm <sup>2</sup> ]	TBD	
Readout Architecture	Asynchronous	TBD
Power [mW/cm <sup>2</sup> ]	< 35	
NIEL [1MeV neq/cm <sup>2</sup> ]	$10^{10}$	
TID [Mrad]	< 10	
Noise [electrons]	< 50	
Fake Hit Rate [hits/s]	< $10^{-5}$ /evt/pix	
Interface Requirements	TBD	

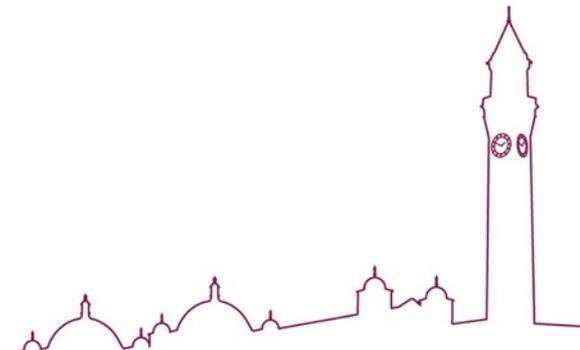
# WP1: DMAPS initial design study

- Study into the readout architecture of an EIC specific DMAPS sensor
  - Starting from the initial specifications
  - Study trade off between pixel size and power density
  - Provide realistic constraints to the detector performance studies
- Strategy
  - First explore most demanding requirements
    - One sensor capable of both tracking/vertexing and time stamping
  - If pixel size and/or power is out of specification
    - Revert to two different chips for tracking/vertex and timing
  - The study splits in two phases: pixel design, readout architecture
- Status
  - Kick-off meeting at the beginning of May followed by monthly meetings
  - Currently looking into pixel analogue front-end design



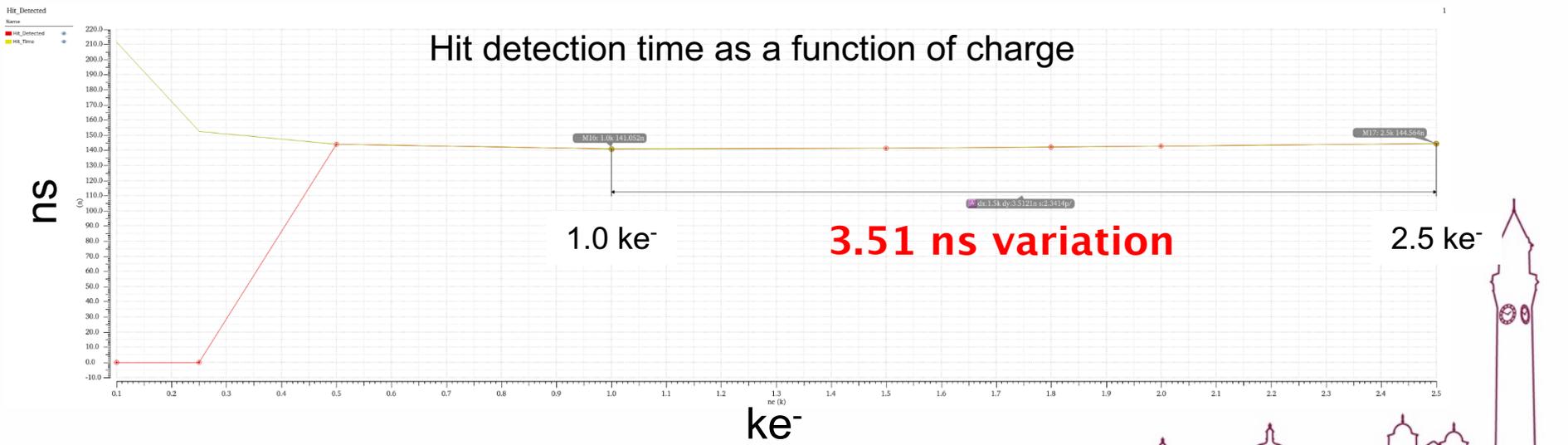
# WP1: Initial simulations of analogue front-end

- The main obstacle to achieve the required time resolution is timewalk
  - Simulated ALPIDE-like FE has 700 ns timewalk for  $Q = 0.5 - 5 \text{ ke}^-$
- Two methods are being investigated to correct for timewalk
- Calibration (as in TimePix3)
  - Little additional circuitry required, FE would be very similar to ALPIDE
  - Calibration procedure needed
  - Timewalk adjusted timing obtained offline
  - ToA and ToT data must both be read out
- Constant fraction discriminator
  - Timewalk adjusted timing is direct output of pixel
  - Only ToA data needs to be read out
  - Complex pixel design



# WP1: CFD simulations

- CFD pixel schematics simulated
  - FE is a simplified version of the ALPIDE FE
- A resolution of approx. 4 ns can be achieved
  - Simulation includes electronics noise
- Power consumption prohibitive for 20  $\mu\text{m}$  pixel pitch (around 2 W/cm<sup>2</sup>)
  - 8 mW/cm<sup>2</sup> with 350  $\mu\text{m}$  pixel pitch
- If this approach is used a dedicated timing layer is needed



# WP1: Information needed to refine specs and simulations

- Several questions need to be answered to define missing specifications and be able to complete the study
- Global and local occupancy
  - Dominated by background hits (follow eRD21 work)
  - Needed to infer acceptable dead time and level of circuitry sharing between pixels
- Expected signal amplitude
  - Currently using  $0.5 - 2.5 \text{ ke}^-$ , with  $1.8 \text{ ke}^-$  being the most probable
- Radiation levels
  - Expected to be low, but need to be quantified
  - If not an issue, SPADS (single-photon avalanche diode) could be a potential alternative technology that would give high spatial and timing resolution with low power

# FY20: Project Proposal

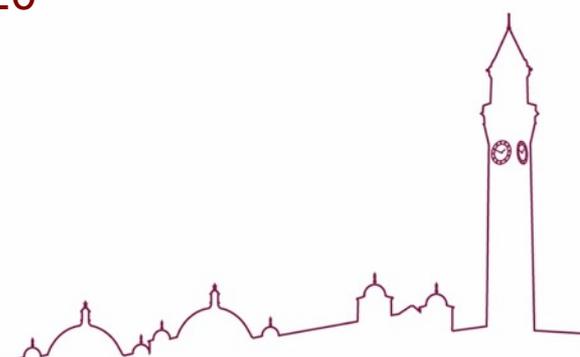
- Bring initial R&D phase to a close and prepare for next phase
  - Design and production of a prototype EIC DMAPS sensor
  - Detector layout optimised for precision measurements of heavy flavour processes and scattered electrons at high  $Q^2$
- WP1
  - Continue to follow evolution of TJ modified process with TJ DMAPS prototypes
    - TJ-MONOPIX (Bonn) available in Q1-2020
  - Conclude EIC DMAPS feasibility study; report to be submitted to the committee in January
- WP2
  - Prepare joint eRD16 and eRD18 report on basic layout simulations
  - Extend simulations to heavy flavour observables

# FY19: Resources Summary

- Awarded: \$72,000
  - Used for travel and chip designer at RAL
  - Equipment descoped; joined test beam data analysis effort of Mini-MALTA

Scenario	Chip designer	Equipment	Travel	Total (USD)
100%	\$60,000	\$6,000	\$14,000	\$80,000
80%	\$44,000	\$6,000	\$14,000	\$64,000
60%	\$24,000	\$6,000	\$14,000	\$48,000

- Remaining funds from FY18 and FY19 committed to design study
  - Study not yet completed, will be carried over to FY20
  - To be completed by end of November
  - Final report will be submitted in January
  - No additional funding requested for this activity



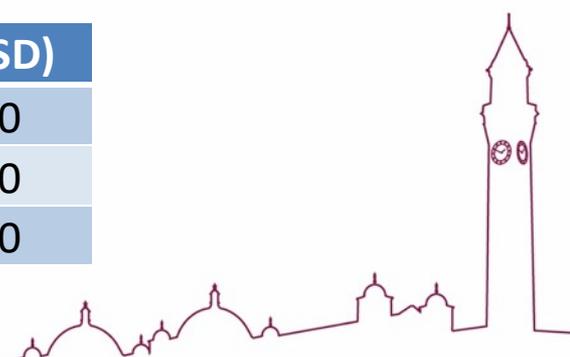
# FY20: Resources Summary

- Existing resources
  - Staff effort: Gonella (0.1FTE), Jones (0.05FTE), Newman, Allport
  - PhD student (Håkan Wennlöf) since October 2017
  - Technology investigations and full detector simulations
  - Access to TJ DMAPS investigator chips and DMAPS prototypes (Bonn)

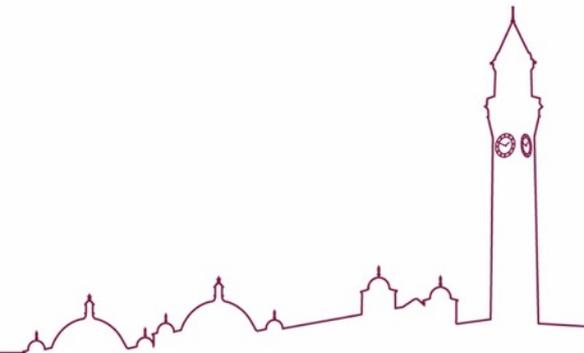
- FY20 funding request

1. DAQ setup for TJ DMAPS prototypes	\$4,000
2. Travel	\$14,000
<b>TOTAL</b>	<b>\$18,000</b>

Scenario	Equipment	Travel	Total (USD)
100%	\$4,000	\$14,000	\$18,000
80%	\$4,000	\$10,000	\$14,000
60%	\$4,000	\$7,000	\$11,000



# BACKUP



# 20x20 $\mu\text{m}^2$

