

# Progress Report: Streaming readout for EIC detectors

Jan C. Bernauer  
for the eRD23 EIC Streaming Readout Consortium

EIC R&D meeting, remote, July 2020



**RBRC**  
RIKEN BNL Research Center



**Stony Brook**  
**University**

# Who are we: SRC members

- ▶ **Brookhaven National Laboratory:** J. Huang, M. Purschke,
- ▶ **Catholic University of America:** S. Ali, V. Berdnikov, T. Horn, M. Muhoza, I. Pegg, R. Trotta
- ▶ **INFN Genova:** M. Battaglieri, M. Bondi, A. Celentano, L. Marsicano, P. Musico, S. Vallarino
- ▶ **INFN Roma:** F. Ameli
- ▶ **Massachusetts Institute of Technology:** D. Hasell, C. Fanelli, I. Frišćić, R. Milner
- ▶ **Stony Brook University:** J. C. Bernauer (also RBRC), E. Cline
- ▶ **Thomas Jefferson National Accelerator Facility:** C. Cuevas, M. Diefenthaler, R. Ent, Y. Furletova, G. Heyes, B. Raydo

Additionally many regulars

→ We welcome new members! ←

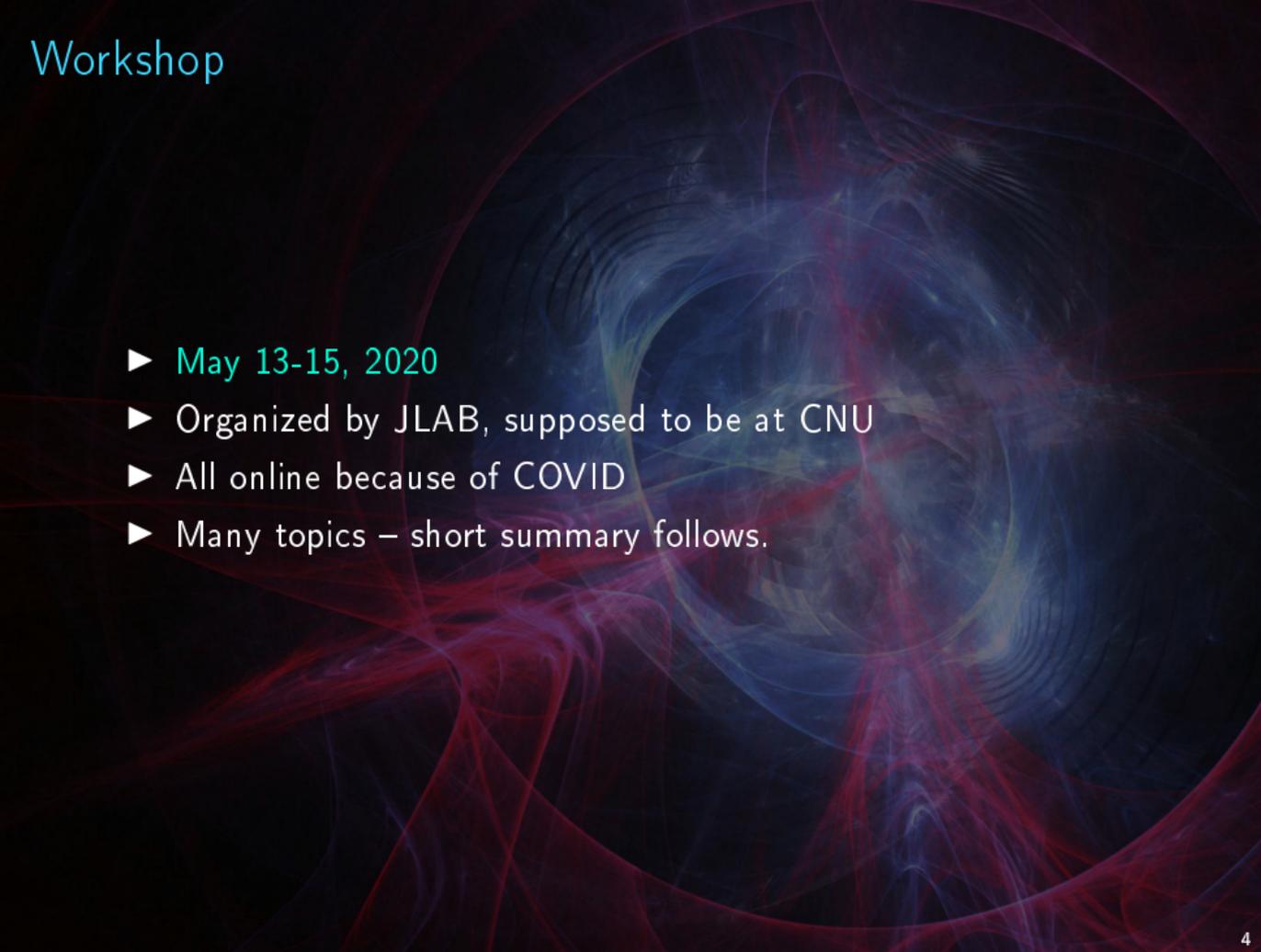
# SRO VI Workshop



Jan C. Bernauer

Chris Cuevas

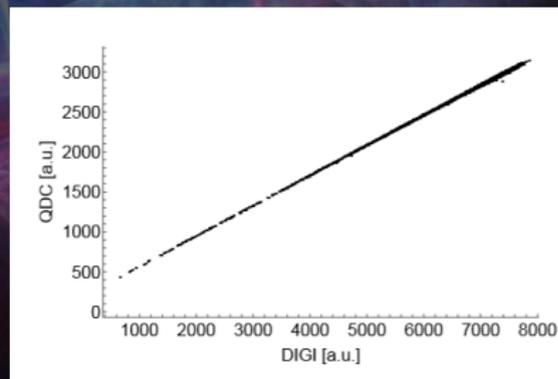
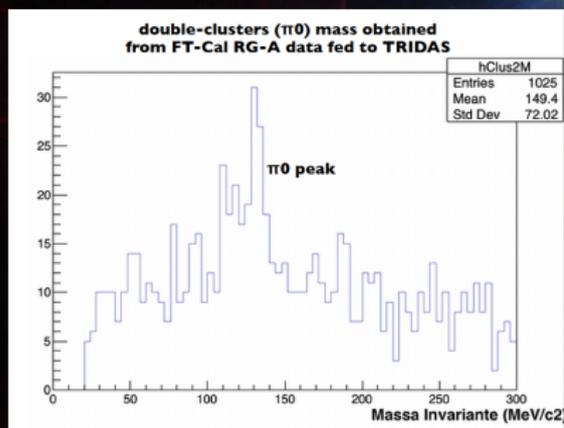
# Workshop



- ▶ May 13-15, 2020
- ▶ Organized by JLAB, supposed to be at CNU
- ▶ All online because of COVID
- ▶ Many topics – short summary follows.

# WS: Beam tests

- ▶ Discussed beam tests at CLAS12 and TPEX.
- ▶ Preliminary results very encouraging.
- ▶ Future beam times planned, work somewhat hampered by COVID.

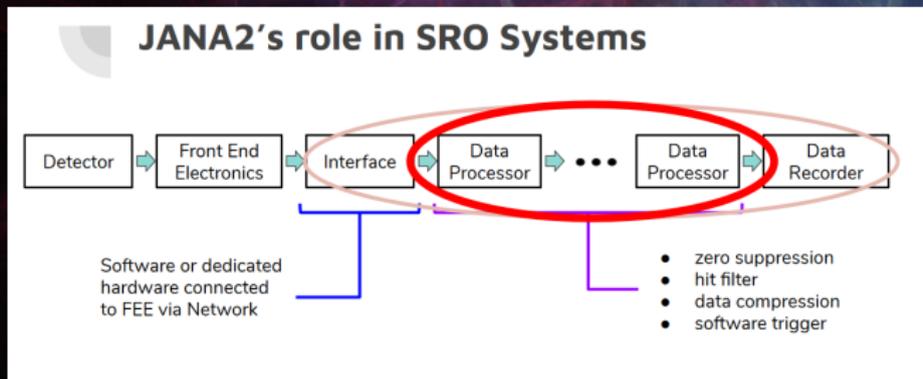


## WS: Electronics

- ▶ Looked at existing ASICs: **TIGER** and **SAMPA**
- ▶ These designs are close to fulfilling our requirements, but might need modifications
  - ▶ sPHENIX & TDIS uses modified SAMPA chips with different shaping time
- ▶ Experts believe timeline for **greenfield** ASIC design will be **ambitious if detector requirements not fixed soon.**
- ▶ But modification of existing designs less time-intensive

## WS: Software

- ▶ Discussed adaptations of "classic" frameworks like **JANA**, **Fun4All**
- ▶ And SRO oriented frameworks like **CLARA**, **TRIDAS**
- ▶ sPHENIX collab. demonstrated streaming-mode analysis
- ▶ Tooling seems to converge on similar ideas. Clear evolution from older designs.
- ▶ Important: Approach needs to be **scalable**, **integrate CPU**, **accelerators nodes**.

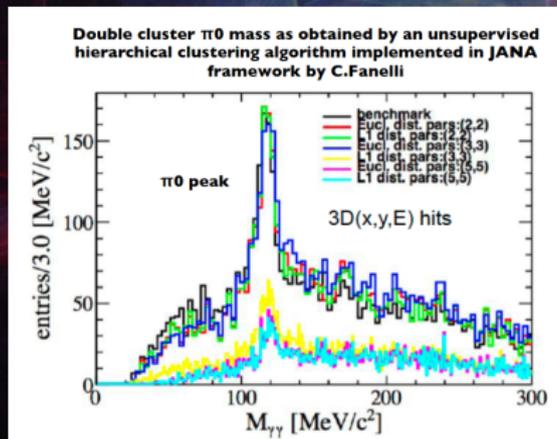


# WS: Transport protocols

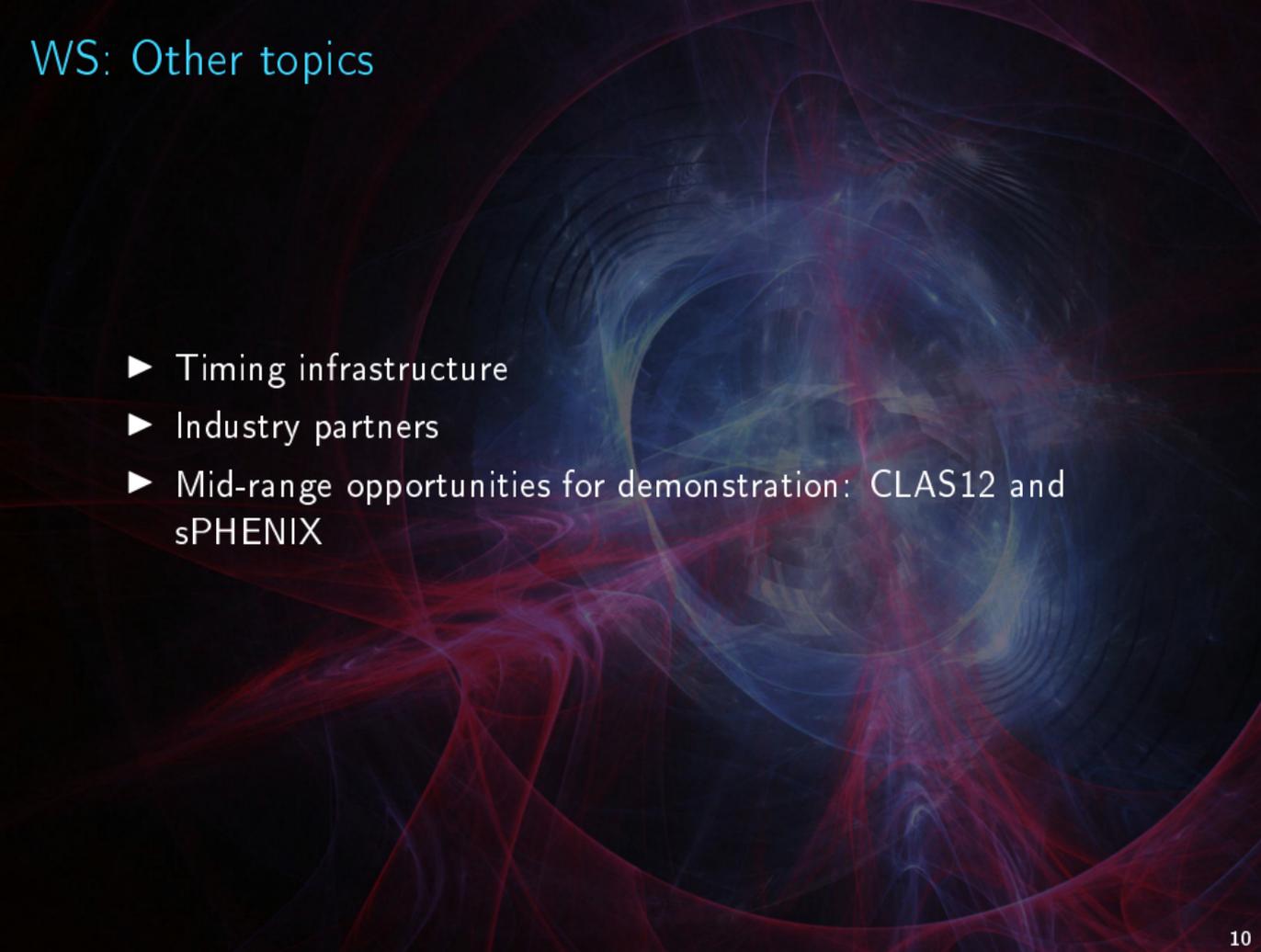
- ▶ Community would like to keep lower-level transport open/flexible
- ▶ Discussed ADIOS as possible general purpose meta-library
  - ▶ Performance lackluster
  - ▶ Leaky abstraction
- ▶ We want to define data-level protocol, further search for transport layer solution

# WS: Machine Learning

- ▶ If online filtering is required, ML might be universal, high-performance solution
- ▶ Can be implemented effectively on FPGA, accelerator IP is available OTS
- ▶ ML algos can outperform classical algos
- ▶ Verification is tricky



## WS: Other topics



- ▶ Timing infrastructure
- ▶ Industry partners
- ▶ Mid-range opportunities for demonstration: CLAS12 and sPHENIX

## Yellow report DAQ meetings

- ▶ Many of us joined the YR DAQ meetings
- ▶ The call of participation was open, not focused on SRO
- ▶ All participants favored a SRO solution.

# Principal guidelines for DAQ I

- ▶ **As much as possible physics agnostic** – should not encode expected physics in its design
  - ▶ time windows, event definition, data selection
- ▶ **Keep as much raw data as possible**
  - ▶ Required reduction depends on detector technology
  - ▶ Current estimate: Complete physics rate can be handled with technology available **now**.
  - ▶ Prefer low-information-loss filters: Cross-detector noise reduction, range-of-interest, time-of-interest data selection
  - ▶ Full reduction to physics objects not required

# Principal guidelines for DAQ II

- ▶ Some detector might need offline calibration
- ▶ At the same time, want to push high-level online or near-online analysis as much as possible
  - ▶ QA
  - ▶ Time-to-publication
- ▶ Noise levels are hard to predict, and might be considerable worse at machine bring-up
- ▶ System needs to be flexible and extensible – later upgrades, additions.
- ▶ Minimize CPU power required in counting room, maximize use of on-site compute
  - ▶ Heterogeneous computing

# Staged bring-up

## Reduce risk at initial commissioning:

- ▶ At the beginning, s/n ratio possibly worse: Mimic traditional trigger with data selection signal from subset of fast detectors.
  - ▶ Not all physics, but enough to learn, get some data on tape
  - ▶ Current technology: Mark time segments in Felix card
  - ▶ But maybe already implemented in software instead of firmware
  - ▶ Simple to implement, low additional overhead

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- ▶ If required, gradually add data filters to reduce data amount, increase event rate
- ▶ At the same time, ramp up online-monitoring.

# Progress at the institutes

The following activities are not funded by eRD23.

## Progress: FADC250 (JLAB)

- ▶ FADC250 and VXS Trigger Processor firmware updated: 4ns timing and int. pulse charge can be transferred to VTP in streaming mode.
- ▶ Tested with 16 FADC250 modules (one crate)
- ▶ Continuing work on zero suppression
- ▶ TCP/IP Stack improved, can saturate 10GBps link

## Progress: EMCAL (INFN, JLAB, CUA)

- ▶ EMCAL instrumented for SiPM readout in streaming mode
- ▶ TRIDAS software for readout in INDRA lab
- ▶ WaveBoard 2.0 for test, later FADC250
- ▶ Will replace PbWO<sub>4</sub> with CUA scintillating glass

## Progress: FT-Cal (JLAB)

- ▶ (Almost) two crate of FADC250 modules for SRO of in-beam experiment.
- ▶ Proof-of-concept with modified TRIDAS.
- ▶ New test planned for August with online algos for data analysis.
- ▶ CODA adaption WIP

## Progress: sPHENIX (BNL, SBU)

- ▶ V5 of SAMPA with 80ns shaping, 20 MHz digitization
- ▶ Better suited for EIC
- ▶ Engineering run delivered, 25 wafer production started
- ▶ Work stopped by COVID. sPHENIX will have three streaming detectors (full tracking system)

## Progress: Timing Module (BNL)

- ▶ New timing system prototype
- ▶ Test if PLL lock can be maintained during RF sweeps of RHIC operation
- ▶ Measure jitter
- ▶ Tests planned as soon as BNL reopens.

## Progress: RFSoc (BNL)

- ▶ Xilinx UltraScale+ RFSoc include multi-gigasamples ADC/DAC
- ▶ Via analog-multiplexing/digital-demultiplexing in frequency domain, can read multiple channels with single ADC
- ▶ Possibility to increase channel-density and reduce analog cable requirements

# Progress: TPEX/DESY test beam (CUA, INFN, JLAB, MIT, SBU)

- ▶ Test beam postponed because of COVID.
- ▶ Analysis of older data is progressing.
- ▶ Will aim to have test beam at JLAB to offset COVID delays.

## Progress: VHDL code for TDC (SBU)

- ▶ Undergraduate project
- ▶ Progressing, but steep learning curve.
- ▶ Student switched to Plasma physics :(
- ▶ Found new student!

## Progress: Collaboration with Alphacore (MIT)

- ▶ Slow because of funding and lack of expertise
- ▶ MIT hopes to hire additional personal after COVID lockdown

# COVID impact

- ▶ Funded work was only slightly impacted – workshop online
- ▶ A lot of unfunded work was strongly affected
- ▶ The funds, allocated for travel, could not be spend.

## Future planned activities

- ▶ Next workshop will likely be at SBU
  - ▶ November
  - ▶ Focus: Initiate definition of data protocol
  - ▶ This will be a continuing project for a subcommittee. Some additional travel for in-person meetings.
- ▶ Test-beams and design process of sPHENIX and CLAS12 will test usability of these standards
  - ▶ CLAS12 SRO test-beams: FT-CAL → Forward Tagger
  - ▶ TPEX test beams at JLAB and DESY

# Funding request

- ▶ We anticipate in-person meetings, test-beam efforts etc will ramp quickly
- ▶ Additional meetings for protocol design
- ▶ Funds also for graduate/undergraduate involvement in test beams etc.
- ▶ Request \$20k

Thank you!



Backup slides

Hic sunt dracones