A triggerless data acquisition system for EM-calorimetry: an R&D activity for the Electron Ion Collider (EIC)

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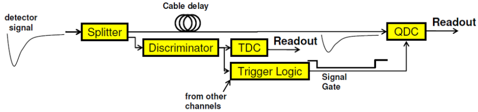
"Traditional" TDAQ systems

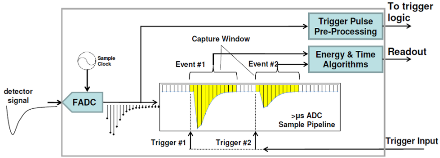
General scheme: data path $\neq$ trigger path

- All channels are continuously measured and hits are stored in a short term "memory" by FEE
- Channels participating in trigger send only partial information to trigger logic ("primitives")
- Trigger logic must take decision in a finite (O(μs)) time - finite memory depth!
- When trigger condition is satisfied:
  - One new, independent "event" is defined
  - Trigger signal is distributed back to FEE boards
  - Data is read from "memory" by DAQ system and stored on tape

"Old-days" memories: delay cables



Modern memories: FPGA-based pipelines



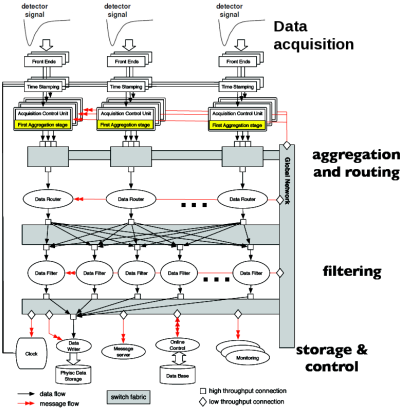
Main drawbacks

- "Primitives" only contain partial event information
- System is difficult to program and debug
- Trigger system can't be modified to cope with different experimental conditions

Triggerless DAQ systems

General scheme: data path ≡ trigger path

Trigger decision is made using **full** information from detector on an online farm of CPUs, connected by a fast network link to FEE



Triggerless DAQ is used by modern experiments: LHCB, Km3, . . .

Technology is available!

- **FEE:** digitizes hits from detector channels, performing minimal processing, and continuously streams them to Hit Manager
- **Hit manager:** receives hits stream from detector subsystem, orders them and sends to TCPU
- **Trigger CPU:** sees the whole detector hits within a finite time-slice. Applies selection algorithms to identify and select events
- **Synchronization:** common clock distributed to FEE boards to provide a time-stamp to each hit

Advantages

- Sophisticated trigger algorithms make use of fully reconstructed and corrected hits
- High-level language implementation
- Easy debug, possibly with MC simulations
- System can be scaled to match different experimental conditions

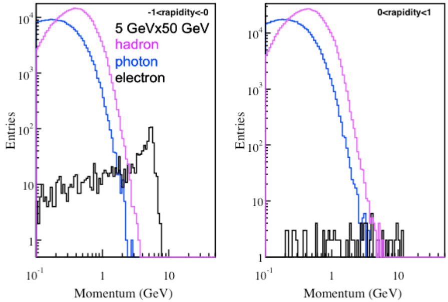
A triggerless system for EIC (1)

A triggerless DAQ provides advantages for all EIC reaction channels

Inclusive channel

- Excellent e' discrimination against hadrons and photons is required
- At large η (large Q^2), low-momentum e' are overwhelmed by hadrons background

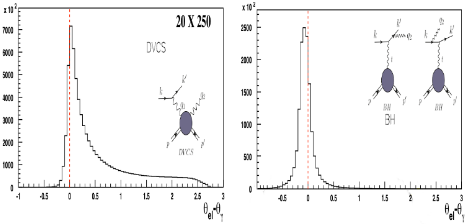
Triggerless DAQ system allows a sophisticated e' selection, making use of advanced algorithms applied to the full information from detector.



Exclusive channel

Several trigger conditions implemented tailored to physics programs. Example: DVCS

- DVCS benefits by the measurement of the hard photon in conjunction with the e'
- The dominant BH background can be rejected by reconstructing θ_e and θ_γ and applying a cut on $\theta_e - \theta_\gamma$



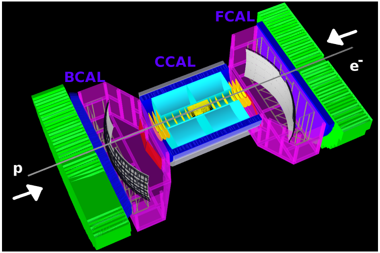
High flexibility to add new triggers for different physics cases!

A triggerless system for EIC (2)

Previous considerations apply to the electromagnetic calorimeter of EIC, **independently** on the technology that will be chosen

TDAQ R&D: why ECAL?

- Full η-coverage calorimeter is part of any optimized EIC detector model
- Calorimeter is one of the key elements of trigger system (e^- identification)
- Results from ECAL TDAQ R&D could be the base for a possible implementation of this strategy to other EIC detectors



TDAQ R&D: why now?

- The use of a triggerless system in EIC needs to be carefully studied in early R&D phase, since it affects the detector design
- CPU/network technology is not affected by "design obsolescence"
- Proposed R&D activity focuses on general system implementation and is not restricted to a specific detector solution

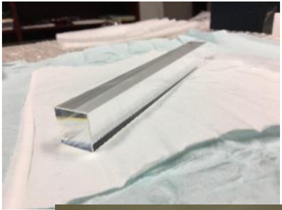
AMD intel

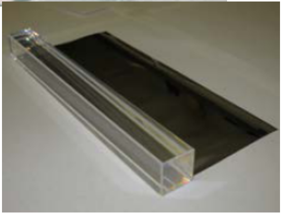
Triggerless DAQ implementation in EIC-ECal: case-study

A realistic implementation of the triggerless DAQ system in a test-case setup is necessary to validate the technology in the EIC-ECal context, understand issues, and demonstrate the expected performances.

A $PbWO_4$ matrix with SiPM readout

- A $PbWO_4$-based calorimeter is the leading choice for e^--side EIC-ECal, being extensively studied within ECAL consortium
- SiPM are a rapidly-growing technology, being investigated for EIC-ECal readout
- Results obtained from R&D activity can be exported to others technologies





Proposed activity outline:

- Implementation of a DAQ system based on a commercial FADC that allows for triggerless readout (e.g. CAEN v1725)
- **Development and test of trigger-less algorithms on a on-line CPU farm**
- Performance comparison with results obtained from a tradional, FPGA-based, triggered DAQ

Proposed R&D activity

Task 1: triggerless readout study

Goal: verify feasibility of triggerless system for EIC-ECal
Activity: setup and characterize a full prototype of front-end / readout / software-trigger chain. Study and implement algorithms to define trigger conditions corresponding to different event topologies (EM showers, cosmic rays, ...)
Prototype response to cosmic rays and light sources will be measured to validate trigger algorithms

Task 2: comparison to triggered readout

Goal: test the same setup instrumented with a traditional, FPGA-based trigger and compare results
Activity: setup a triggered setup using JLab state-of-the-art trigger boards, implementing trigger algorithms on FPGAs

Task 3: optimized FE board for EIC-Ecal

Goal: design a FE board (block-diagram) that integrates the discrete components tested during the previous activity

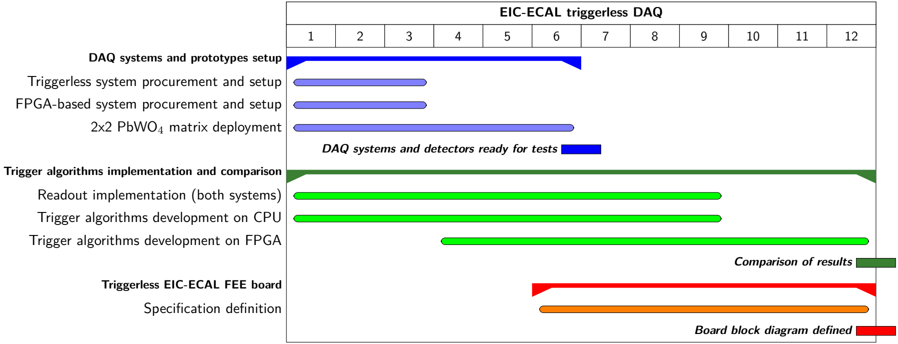
CAEN v1725

JLab fADC250

Time-schedule, deliverables and budget requests (1)

Project time-schedule:

- Hardware and software tasks have been clearly distinguished, since will be in charge of different people, working together under PI supervision
- Three milestones, set in the middle and at the end of the 1-y term, allow the project reviewers to check progresses



If funded for another term, the follow-up of this activity will include the on-beam tests of one or more prototypes developed by other consortium members and the construction of a triggerless modular acquisition board.

Time-schedule, deliverables and budget requests (2)

To achieve the proposed R&D program, we are mainly accounting on resources (equipment/personell) funded by INFN.

- INFN-Genova involved people: 6 scientists, 1 PhD student + support from electronics department
- Already-available equipment: $PbWO_4$ crystals, VME-VXS crate, HV, LV
- Equipment that will be procured with INFN funds: SiPMs, CPU-server, high performance network switch

Total INFN contribution: 50 k$, equipment only

Budget request:

Item	Cost
Caen V1725 digitizer	10 k$
Consumables	2 k$
Travel funds	6 k$
Personell: 1-y post-doc	40 k$

- 20% budget-cut scenario: V1725 → V1720 (8 ch, 12 bit)
- 40% budget-cut scenario: N/A due to quantization of post-doc support

The post-doc primary responsibility is the study of triggerless algorithms, the development on CPU, and the experimental measurements, working at INFN-Genova under PI supervion. INFN / JLab staff is in charge of hardware activity (DAQ systems and prototype setup)

Conclusions

- We propose an R&D activity focused on the study of a triggerless DAQ system for EIC-ECal
  - Whole EIC program will benefit from this system, that allows to implement sophisticated event-selection algorithms within an high-level framework, making use of full reconstructed information from detector
- Test-case implementation of ECAL triggerless system: 2x2 array of $PbWO_4$ crystals read by SiPM
  - DAQ performance will be tested with cosmic rays and light pulser will be measured
  - We'll compare performances obtained from a triggerless system to a traditional, FPGA-based, readout
- R&D project is mainly based on instrumentation and equipment funded by INFN ($\simeq$ 50k$ investment)
  - Budget request mainly driven by a post-doc support for 1 year
  - Post-doc will follow software implementation of triggerless system and will be in charge of measurement campaign and comparison with triggered system

Backup slides

EIC-Ecal rates estimate

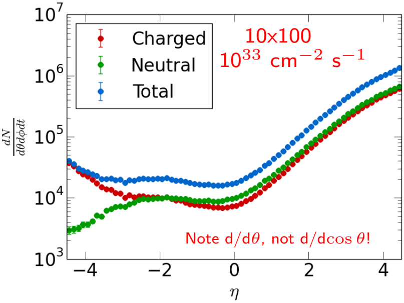
Electron-side $PbWO_4$ calorimeter:

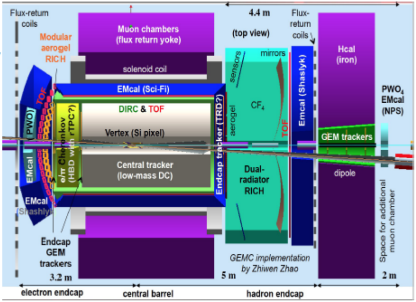
- $\eta \simeq -4$, $R_{tot} \simeq 9 \cdot 10^6$ Hz/srad @ 10^{34} cm$^{-2}s^{-1}$
- Considering 2x2 cm^2 crystals at $\simeq$ 2 m from IP, $\Omega \simeq 10^{-4}$ srad
- R$_{single} \simeq 900$ Hz, x8 due to EM showering from neighborhoods $\rightarrow \simeq 10$ kHz

Hadron-side very-forward calorimeter ($PbWO_4$):

- $\eta \simeq 4$, $R_{tot} \simeq 3 \cdot 10^8$ Hz/srad @ 10^{34} cm$^{-2}s^{-1}$
- Considering 2x2 cm^2 crystals at $\simeq$ 7 m from IP, $\Omega \simeq 8.1 \cdot 10^{-6}$ srad
- R$_{single} \simeq 2.5$ Hz, x8 due to EM showering from neighborhoods $\rightarrow \simeq 20$ kHz

Very preliminary calculations!





Proposed R&D activity (1)

The activity is composed by 3 tasks: study of the triggerless readout, comparison to an FPGA-based trigger option, and development of an optimized FE board matched to the EIC-ECal specifications

Task 1: triggerless readout study

Goal: set-up and characterize a full prototype of front-end / readout / software-trigger chain.
Activity:

- Instrument a 2x2 $PbWO_4$ crystal array with SiPMs (6x6 mm^2)
- Setup the digitizer (CAEN V1725) in streaming-mode, transferring data from single channels when (local) threshold crossing occurs.
- Develop DAQ system to read the datastream, writing Hit Manager and TCPU software.
- Study and implement algorithms to define trigger conditions corresponding to different event topologies (EM showers, cosmic rays, . . .)

Prototype response to cosmic rays and light sources will be measured to validate trigger algorithms

Proposed R&D activity (2)

Task 2: comparison to triggered readout

Goal: test the same setup instrumented with a traditional, FPGA-based trigger and compare results

Activity:

- Setup a TDAQ system based on the JLab fADC250 VME-VXS board, using VTP board for triggering, and CODA2.0 software for system management
- Implement trigger algorithms on the FPGA hosted in the VTP board
- Compare performance and results

Task 3: Optimized FE board for EIC-Ecal

Goal: design a board (block-diagram) that integrates the discrete components tested during the previous activity, adopting a modular layout to adapt to different photo-sensors by implementing analogue front-end on interchangable mezzanines.

JLab fADC250

JLab VTP