Low-Mass Silicon Pixel Sensor with In-Pixel Readout Electronics for EIC Tracking and Vertexing

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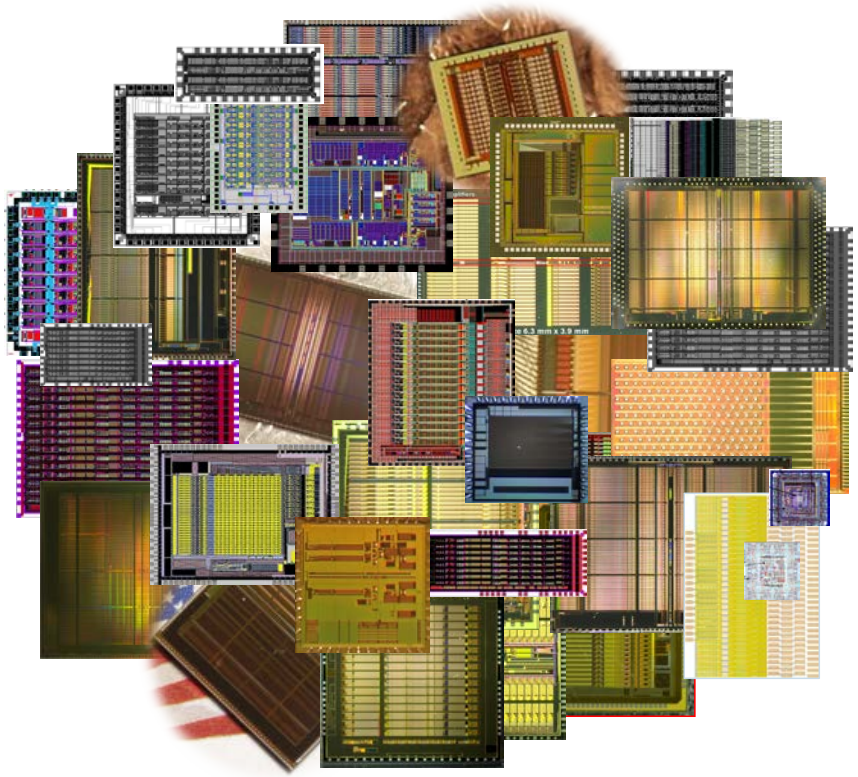

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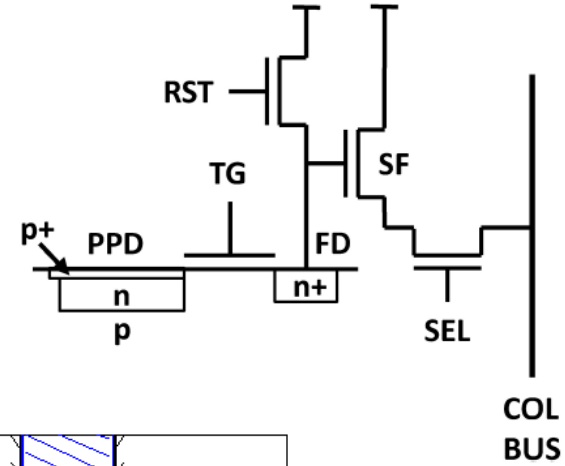
Outline

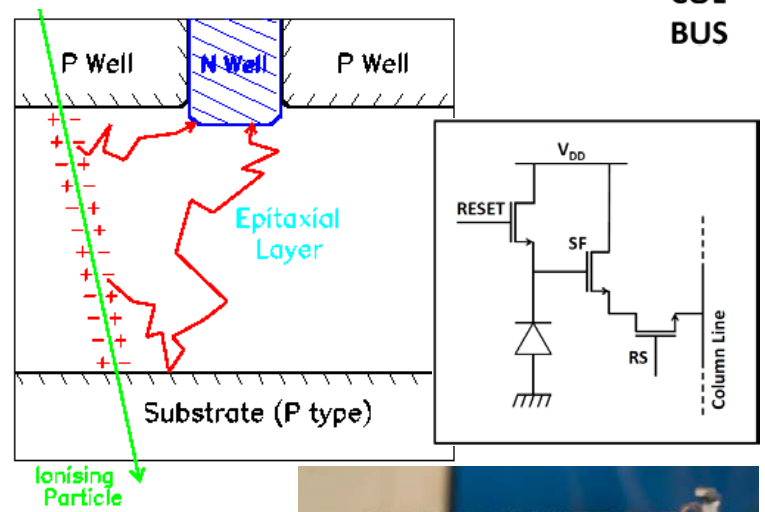
- **Review of state-of-the-art Monolithic Active Pixel Sensor (MAPS) technologies**
- **Motivation and technical advantages of the proposed low-mass sensor with in-pixel readout electronics for EIC tracking and vertexing**
- **Collaborations**
- **Next steps**

Introduction

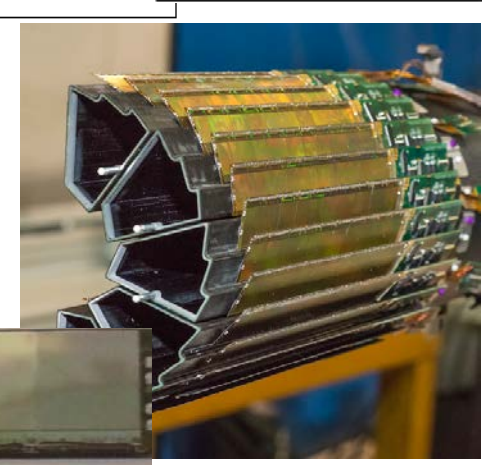
- CMOS Active Pixel Sensors (APS) were invented by Fossum et al. at JPL in 1993, now used commonly in camera phones, webcams, DSLRs, etc. They include a Pinned Photo-Diode (PPD) to collect charge, and a very simple "**rolling shutter**" in-pixel circuitry (3 or 4 transistors). The fill factor is about 20~30 %.



- In 2001, Turchetta et al. at Strasbourg proposed an n-well/p-substrate diode to achieve 100% fill factor, called Monolithic Active Pixel Sensors (MAPS), and later was applied for the STAR Heavy Flavor Tracker. Charge is collected mainly by diffusion in the epitaxial layer.

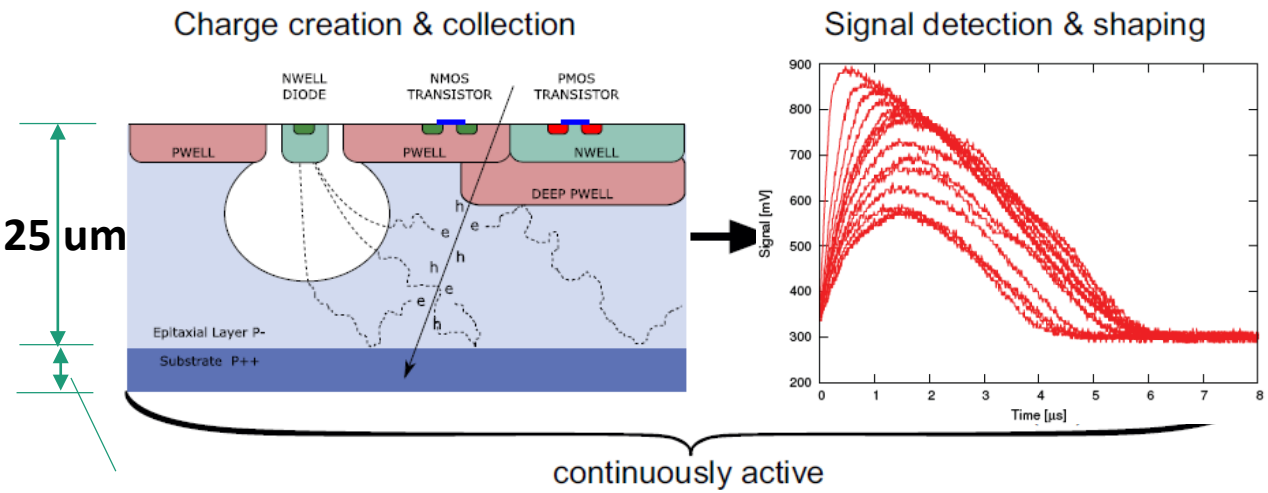


STAR HFT PXL detector:
Ladder with 10 MAPS sensors (~2 × 2 cm each)
[Cortin_JINST2015]



State-of-the-Art MAPS Technologies (1): ALPIDE

Standard CMOS Image Process (TowerJazz 180nm) [Snoeys et al._ JINST2013]



Issues:

Electronics: **coarse shaping** at 40nW/pixel

-> time resolution: **>30 us**

-> detectable charge: **>130 e-**

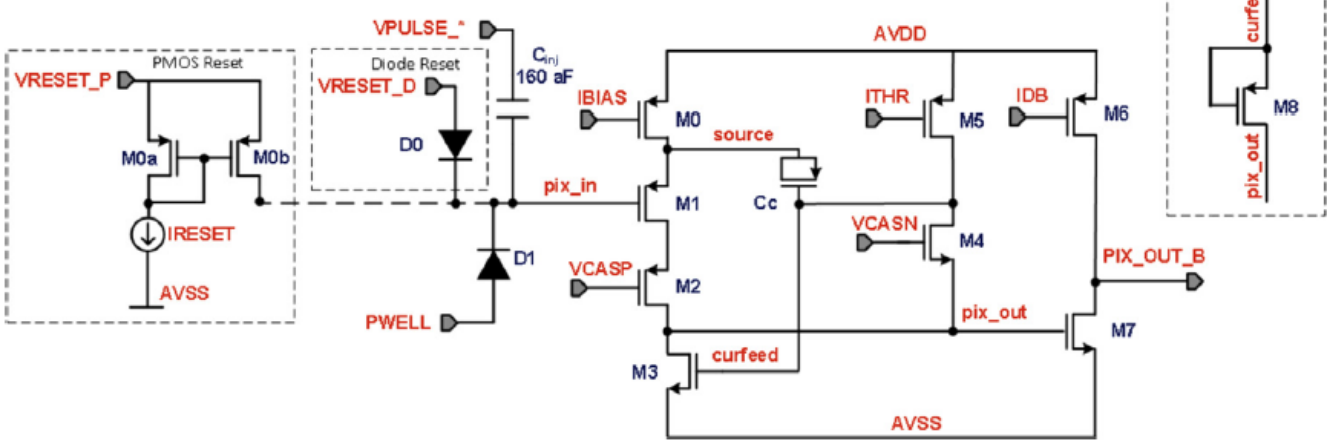
Sensor: **charge loss** by trapping

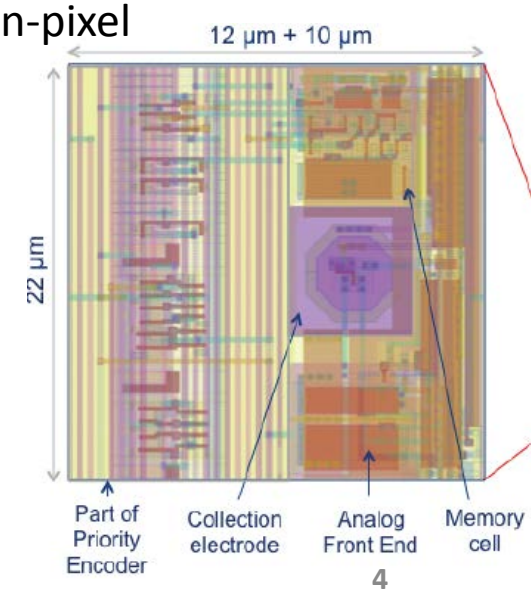
-> improve by depletion (in DMAPS/HV CMOS)

thinned from ~250um to ~25um

A major advantage: **in pixel front-end electronics (amplification and discrimination)**

(Most commonly adopted 3/4 T MAPS technologies do not have such in-pixel readout electronics, and need external readout electronics!)

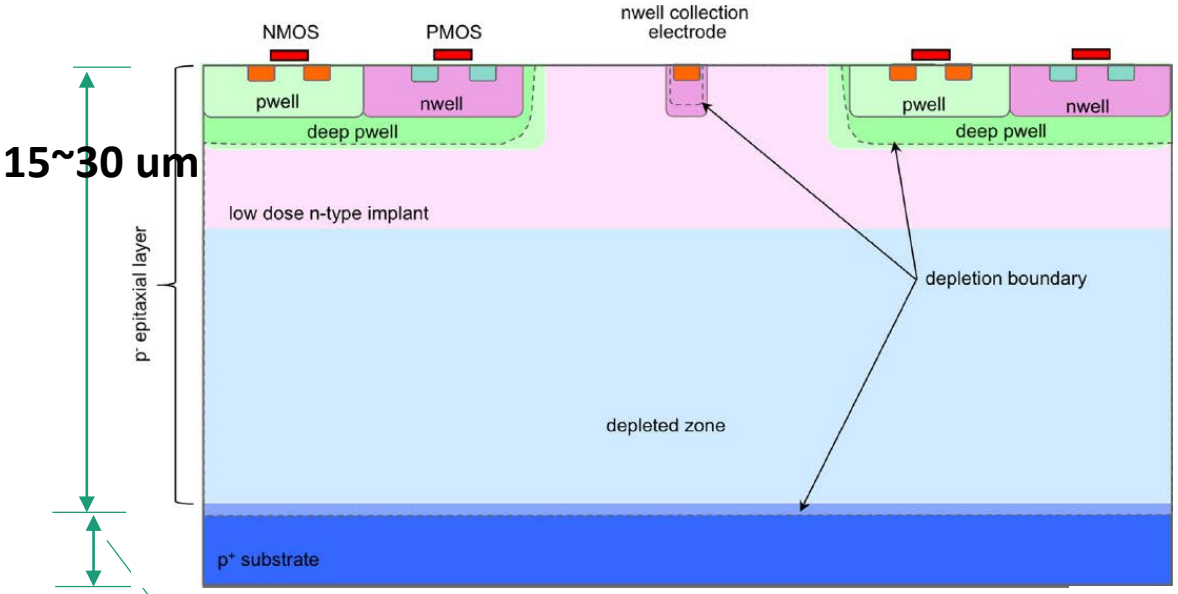




State-of-the-Art MAPS Technologies (2): DMAPS

Depleted CMOS Image Process (TowerJazz 180nm):

[Snoeys et al._NIMA2017]



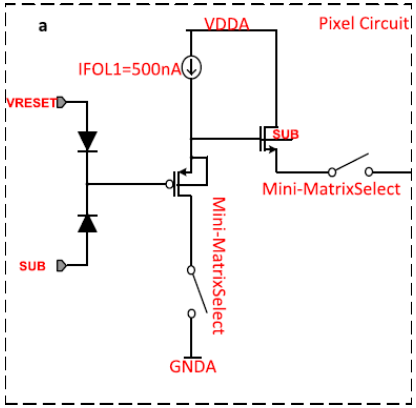
thinned from ~250um to ~25um?

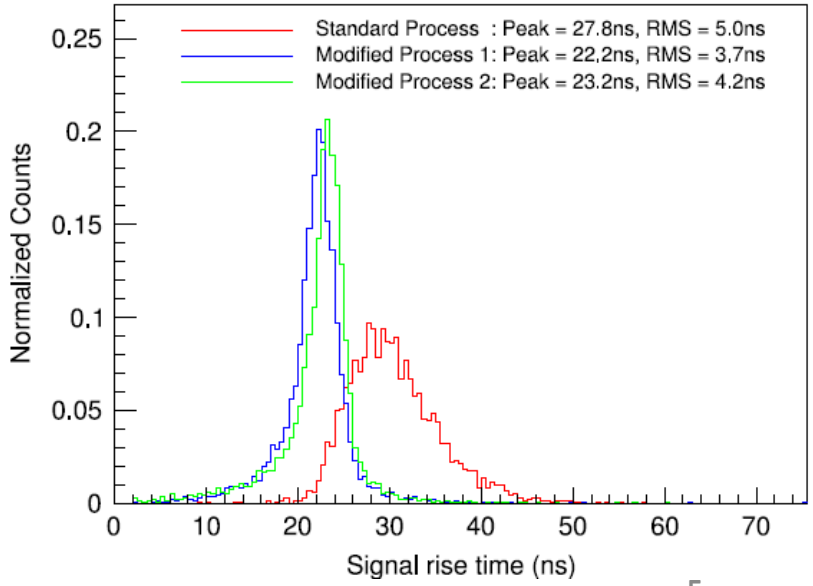
Does NOT include in-pixel front-end electronics

-> bump-bonded to FE-I4 front-end pixel readout ASIC w/ a pitch of 33um x 125um, ~300um thick

A low-dose n-type implant is reverse biased (~10V) to full depletion:

-> to **improve signal rise time** in the sensor

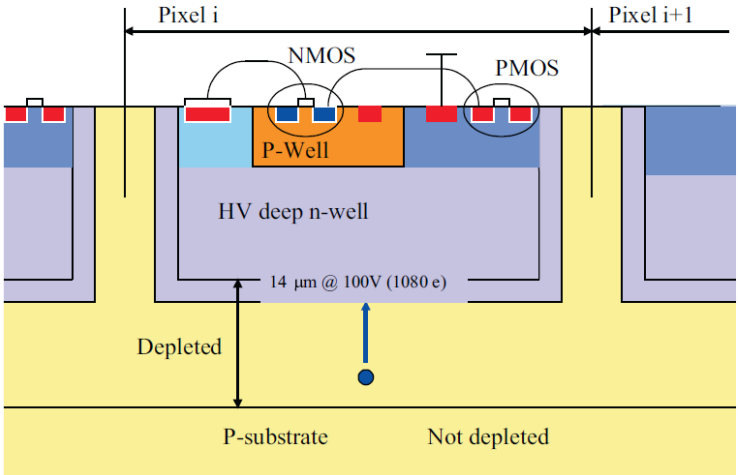




State-of-the-Art MAPS Technologies (3): HV CMOS

HV CMOS Process (AMS 350nm/180nm)

[Peric et al._NIMA2011]

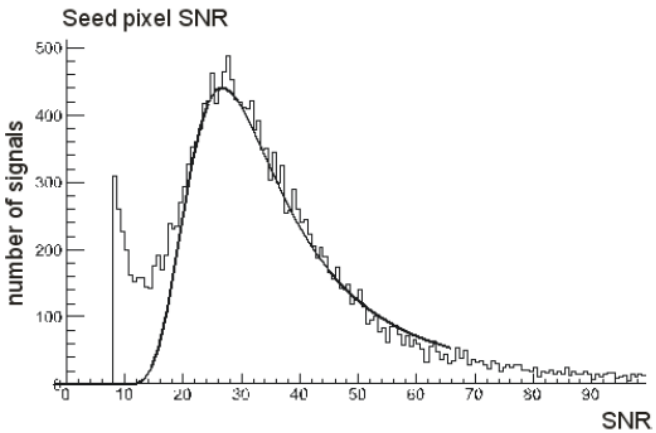


Reversely bias the deep n-well ~100V:

-> fast charge collection by drift

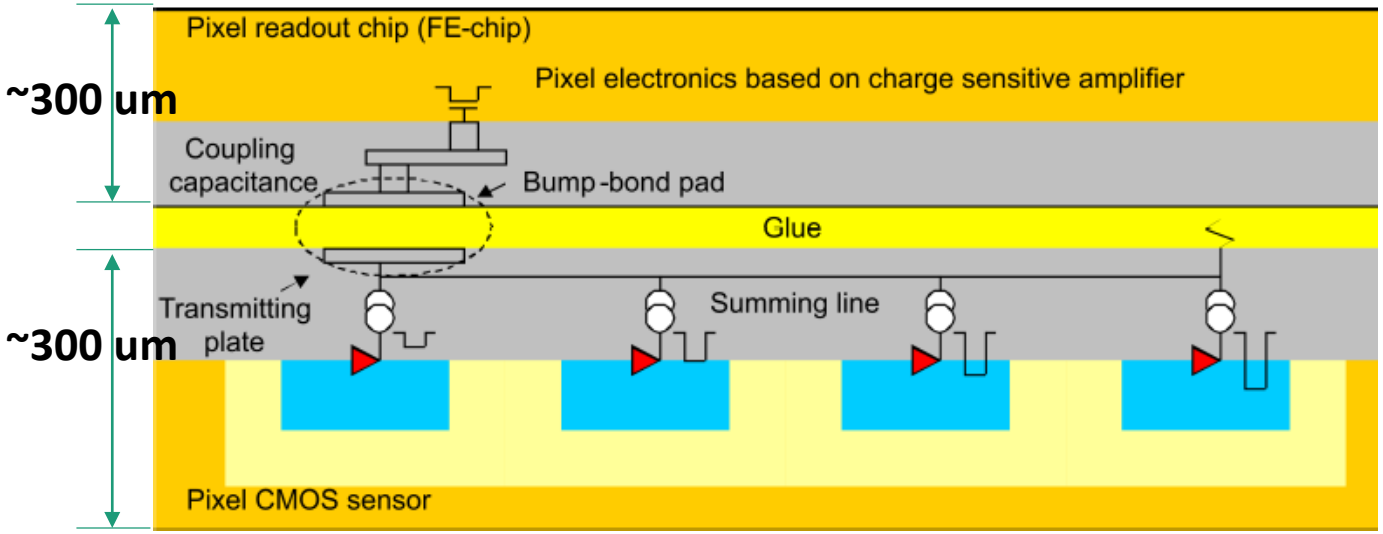
(~40ps in theory, limited by in-pixel elec. to ~40ns)

-> improve sensor SNR



Include very simple in-pixel electronics: CSA and comparator

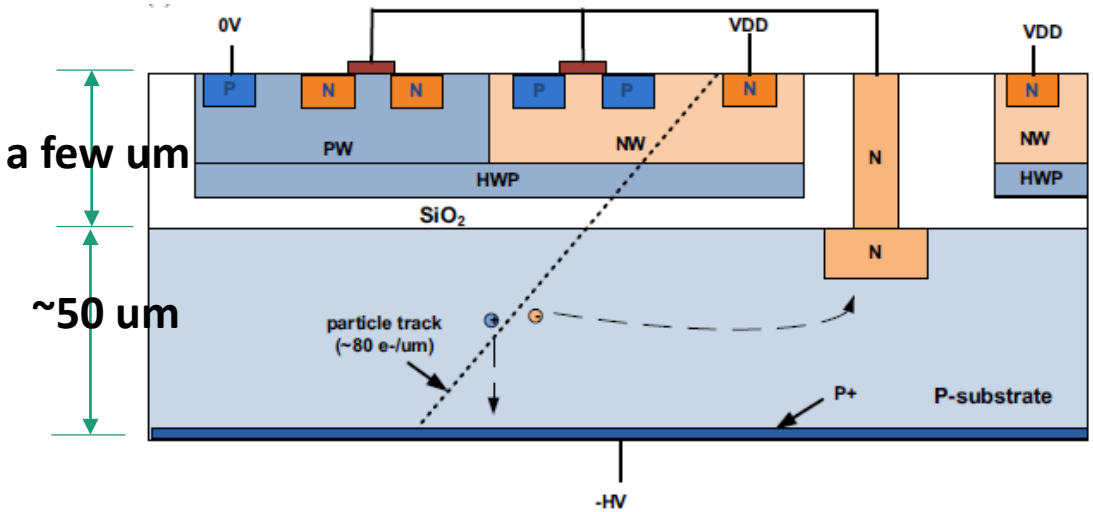
-> bump-bonded to FE-I4 front-end readout ASIC w/ a pitch of 33um x 125um)



State-of-the-Art MAPS Technologies (4): HV SOI

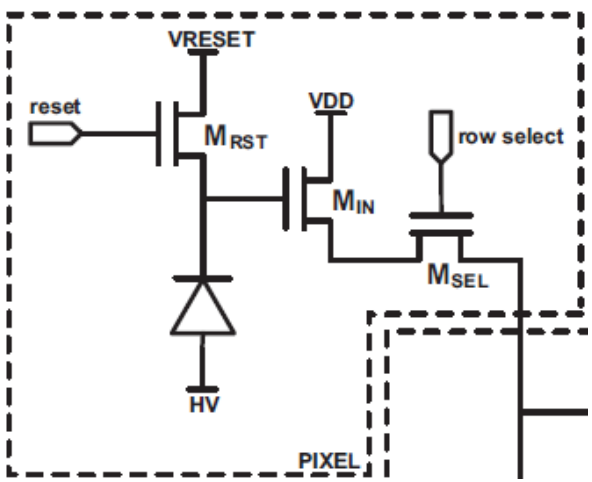
HV Thick-Film SOI Process (XFAB 180nm)

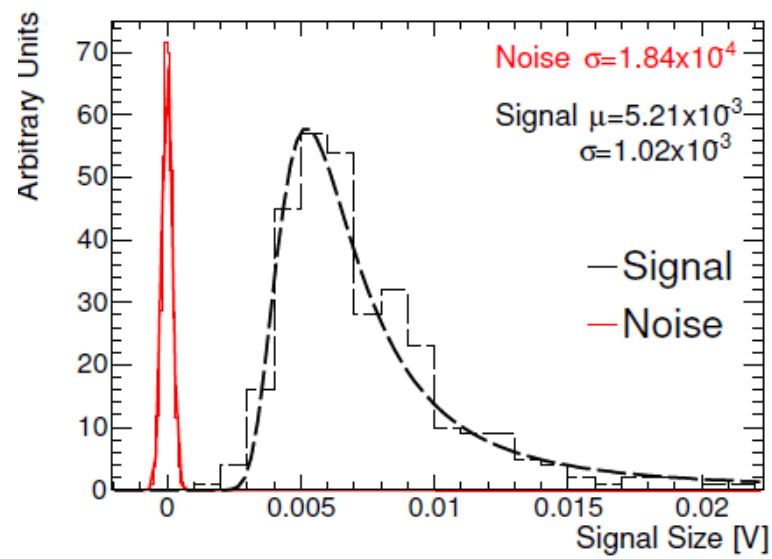
[Hemperek et al._NIMA2015]



- **Thick SOI (a few um vs. tens of nm in regular SOI)**
  -> improved radiation hardness (~700 Mrad)
- **Use the inactive handling wafer (~50 um) as depleted sensor, reverse biased ~150V**
  -> SNR ~ 22

Does NOT include in-pixel front-end electronics, only the 'rolling shutter' 3T readout; tested with FE-I4 readout ASICs.



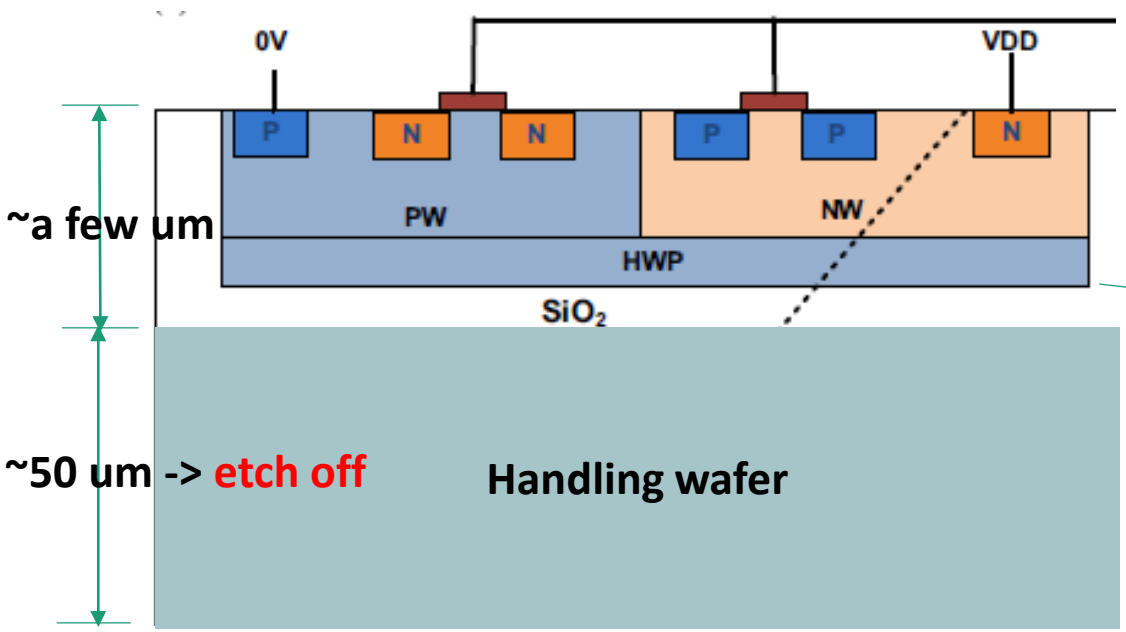


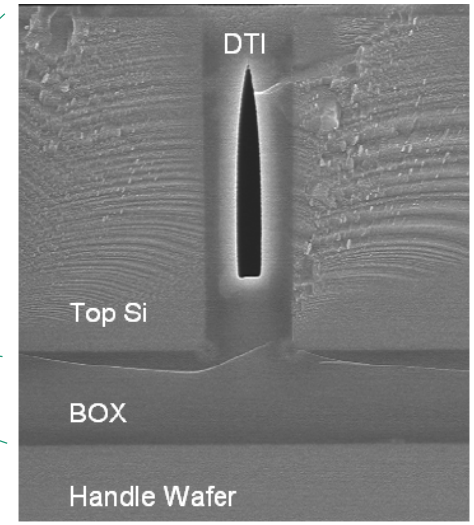
Limitations of the State-of-the-art MAPS Technologies

	ALPIDE [ALICE ITS upgrade]	***DMAPS*** [ALICE ITS upgrade]	***HV2FEI4*** [ATLAS upgrade]	***XTB01/02*** [ATLAS upgrade]
Technology	**CMOS Image Process** (TowerJazz 180nm)	**Depleted CMOS Image** (TowerJazz 180nm)	**HV CMOS** (AMS 350/180nm)	**HV Thick-Film SOI** (XFAB 180nm)
Pixel size	30 µm x 30 µm	30 µm x 30 µm	33 µm x 125 µm	50 µm x 50 µm
Pixel electronics	Sensor/preamp/ shaper/discriminator	Sensor only **->need readout ASIC**	Sensor/preamp/comp **->need readout ASIC**	Sensor only **->need readout ASIC**
Thickness	thinned to ~50 µm		~ 300 µm (standard)	~50 µm
Electron collection time	100 ns		40 ps in theory limited by elec. to 40ns	150 ns
Integration time	30 µs		400 ns (FE-I4 shaper)	
Spatial Resolution	5 µm	9 µm	~3 µm	15 µm
TID	3 Mrad	1 Mrad	50 Mrad (analog) 10 Mrad (discrimator)	< 700 Mrad
NIEL	2×10^{13} n_{eq}/cm^2	10^{15} n_{eq}/cm^2	10^{16} n_{eq}/cm^2	5×10^{13} n_{eq}/cm^2
Bias Voltage	< 10 V	< 10 V	< 100 V	< 300 V
SNR	< 33	33	27	22
Readout rate	**100 kHz**		40 MHz (FE-I4)	
Power	40 nW/pixel (analog) 40 mW/cm^2 (90% dig.)		**7 µW/pixel**	-

Motivation (1): Low Mass -> Thinned SOI Process

- Post-process the thick-film SOI:
  - **thin the silicon to only a few um**, by etching off the entire handling wafer (~50 um)
  - use the Buried OXide (BOX), i.e. SiO_2, as a **supporting material**
  - use the BOX layer as a **natural etching stopper** for uniformity





A partial cross-section SEM image of X-FAB SOI 180nm [Holke_ISPSD2010]

Motivation (2): Low Mass -> In-Pixel Readout Electronics

- Integrate sensor with in-pixel readout electronics
-> to **reduce mass of external readout ASICs**
- Develop **low-noise front-end amplification, shaping, and discrimination** with 10~20 transistors in 20um x 20um pixel-very challenging!
- Target **shaping time < a few tens of ns**, to differentiate between particle bunches
- Allocate analog power > 40nW/pixel for low-noise amplification and fast shaping
-> how much can we allocate?
- Lower digital power in common digital processing to achieve < 40mW/cm^2
-> need realistic power budget from detector R&D

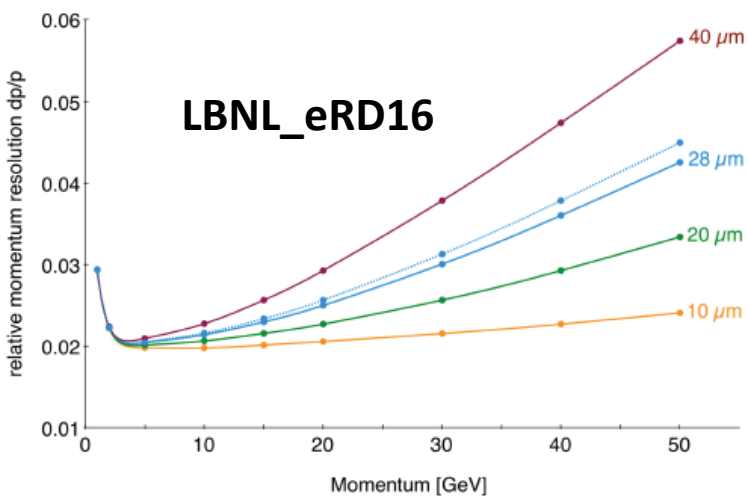
Proposed Specifications for the Low-mass Sensor w/ in-Pixel Readout Electronics (tentative)

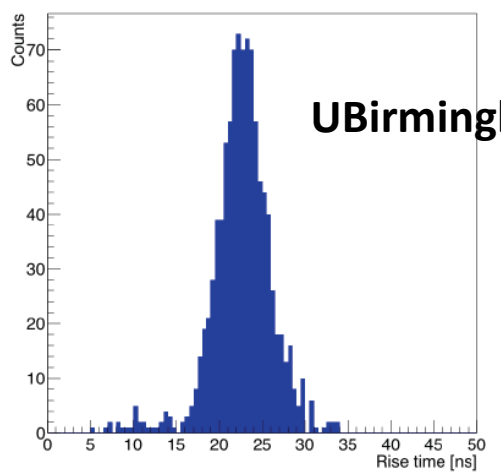
Detector Requirements	Target Specifications	Priority
Pixel pitch	~20 µm	High
Sensor SNR	> 30	Low
In-pixel shaping time	**< a few tens of ns**	Medium
Radiation dose	~ 250 rad/yr	Low
Neutron flux	~ 10^{10} $n_{eq}/cm^2/yr$	Low
Readout rate	50kHz - 10MHz	?
Power	< 40 mW/cm^2	?
Low mass	Integrated sensor AND readout electronics on thinned SOI -> **a few µm**	High

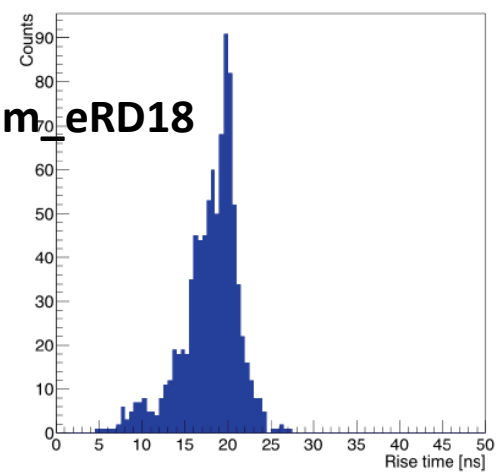
[Kiselev_EICUG_Nov2017 & Aschenauer et al._acXiv2014]

Collaborations

- We need **close collaboration with the EIC community** for inputs of detector specifications to optimize the sensor and electronics design to achieve low noise, fast readout at very low power.
- We hope for frequent conversations with **EIC silicon groups** for technical discussions and exchanges of R&D results (very helpful!) to proceed efficiently.
- Also collaborate with BNL NSLS-II (Siddons et al.) for Cyro-EM & UED, on testing the low-mass SOI concept.
- Currently collaborate with a commercial foundry, X-FAB, on the SOI process.







Next Steps

- Test the **low-mass SOI concept** on commercial SOI wafers.

- Develop **back-contact** on thinned SOI wafer for depletion in Instrumentation's clean room.

- Develop and characterize different **photodiode architectures** (within a few um) on thinned SOI wafer and measure dark current in Instrumentation's Detector group.

- Develop **in-pixel readout electronics** upon selected SOI technology and study of detector specifications in Instrumentation's Microelectronics group.

- Characterize prototype low-mass sensor with in-pixel readout electronics with particle and ion beams, in collaboration with the EIC community.

Backup Slides

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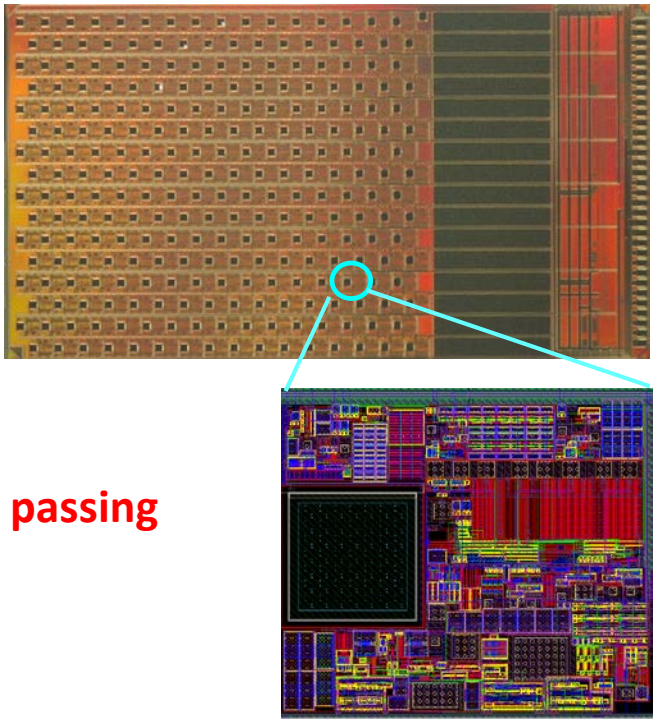
Review of ASICs Developed at BNL

Year	ASIC Families	Collaborator	Publications	Impact areas
1996-1999	ATLAS family	ATLAS	*	Particle Physics
1996-1999	RHIC family	RHIC	*	Nuclear Physics
1997-2001	CreV family	eV Products	*	Nonproliferation, Medical Imaging
2000-2004	HERMES family	NSLS	*	Energy Sciences, Light Sources, Medical Imaging
2001-2009	PDD family	eV Products	*	Energy Sciences, Light Sources
2002-2003	CPG1 ASIC	LANL	*	Nonproliferation
2003-2004	LEGS TPC ASIC	Physics	*	Nuclear & Particle Physics
2005-2008	CPG2 ASIC	eV Products	*	Nonproliferation
2005-2007	SNS He^3 ASIC	ORNL	*	Energy Sciences
2005-2007	Multiwindow ASIC	eV Products	*	Nonproliferation, Medical Imaging
2005-2008	RATCAP ASIC	Medical	*	Medical Imaging, Neuroscience
2006-2011	H3D family	DoD, UMich	*	Nonproliferation, Medical Imaging
2006-2009	Compton Imager ASIC	NRL, NASA	*	Nonproliferation, Energy Sciences
2006-2010	LUNAR family	NSLS, NASA	*	Energy Sciences, Light Sources
2010-	DUNE front-end ASIC	Physics	*	Particle Physics
2011-	DUNE ADC ASIC	Physics	*	Particle Physics
2011-	ATLAS VMM family	Physics	*	Particle & Nuclear Physics
2014-	MARS family	NSLS	*	Energy Sciences, Light Sources
2014-	HEXID 2D family	NSLS, NASA, SBU	*	Energy Sciences, Light Sources
2015-	Ge family	LBNL, LANL	*	Particle Physics, Energy Sciences, Nonproliferation
2015-	H3DD family	DoD		Nonproliferation, Particle & Nuclear Physics
2015-	ATLAS HLC ASIC	Physics	*	Particle Physics
2016-	SAR ADC ASIC	Physics		Particle Physics, Energy Sciences
2016-	LDO regulator	Physics		Particle Physics, Energy Sciences

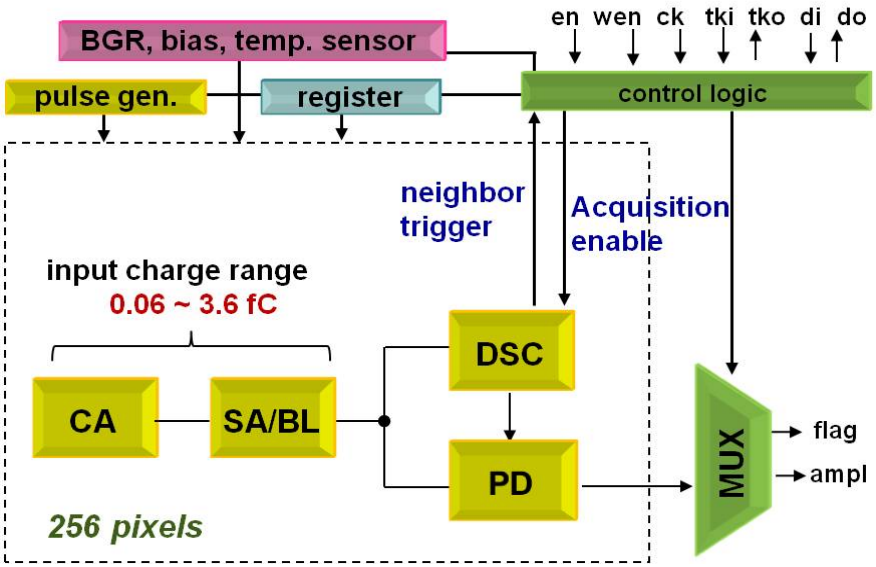
2-D ASIC Hi-Resolution X-ray Imager

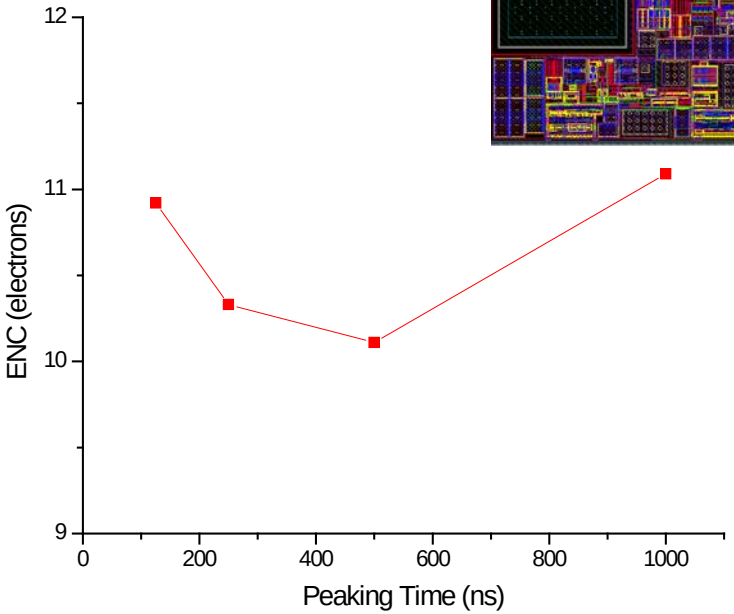
- ~700,000 transistors in CMOS 130nm technology (1.2 V supply)
- 256 hexagonal channels at 250 µm pitch
- 3-side abuttable, with 33 I/O pins only on the right side
- Each channel includes:
  - -low-noise charge amplifier (adjustable gain: 0.25, 0.5, 1 V/fC)
  - -shaper (adjustable peaking time: 125, 250, 500, and 1000 ns)
  - -baseline stabilizer
  - -discriminator and peak-detector
- ~0.6 mW/channel
- Simulated ENC: ~ 11 electrons (@ 60 fF det. cap. & 6pA leakage per pixel)



⇒Limited area for low-noise low-power readout chain

⇒No direct address control of each pixel, relying on token passing

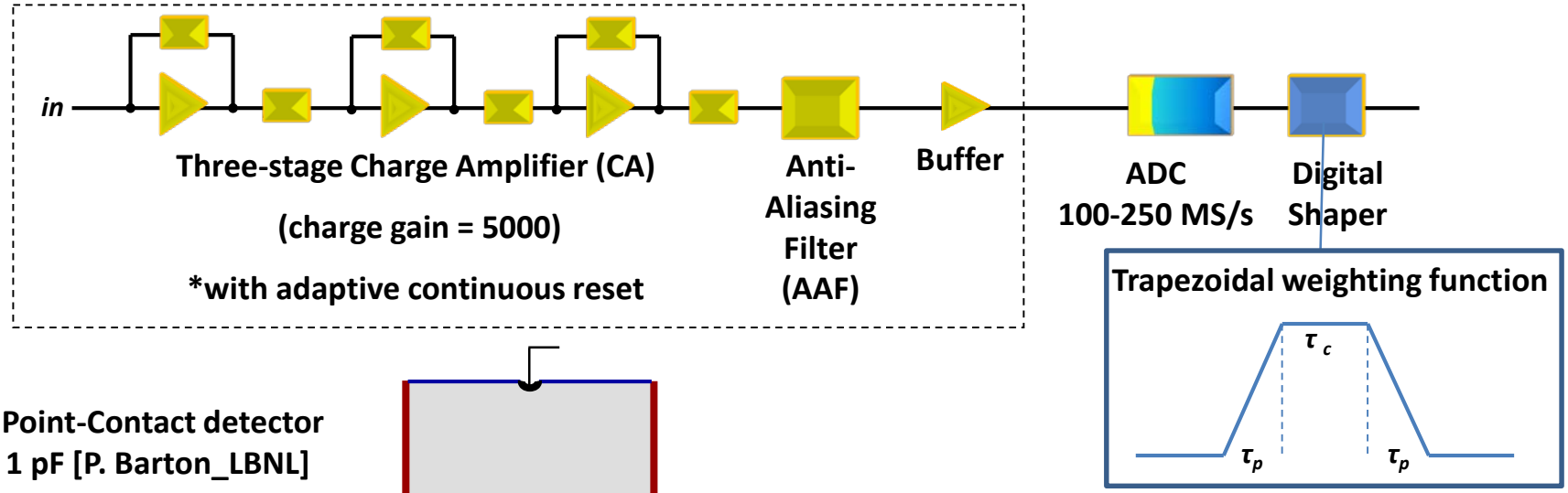




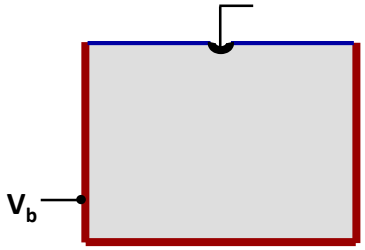
[S. Li et al., IEEE NSS 2017]

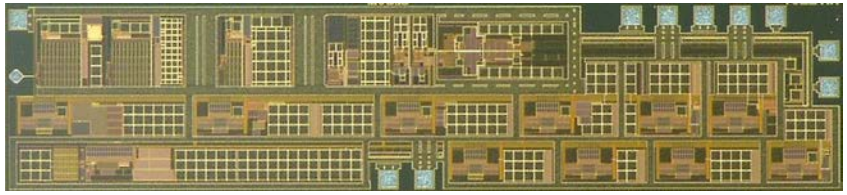
Very Low Noise ASIC for Germanium Point-Contact Detector in LAr

- **Large gain** (~5000) of charge amplifier to lower noise contributions from later stages
- **Adaptive continuous reset** successfully avoid dead-time and switching noise in charge amplifier, and automatically adjusts to detector leakage current.
- **Large bandwidth** of anti-alias filter (AAF) to preserve 50ns pulse rise time



Ge Point-Contact detector
C < 1 pF [P. Barton_LBNL]





Cdet (fF)	ENC_total (e-)	ENC _m1&lk (e-)	ENC_m1-1/f (e-)
200 (possible load)	5.3	4.8 (~82%)	4.5 (~71%)
100 (target load)	**3.9**	3.5 (~78%)	3.2 (~65%)
1 (**without load**)	**2.6**	2.1 (~68%)	1.9 (~48%)

[S. Li et al., IEEE NSS 2017]

SAR (Successive Approximation Register) ADC

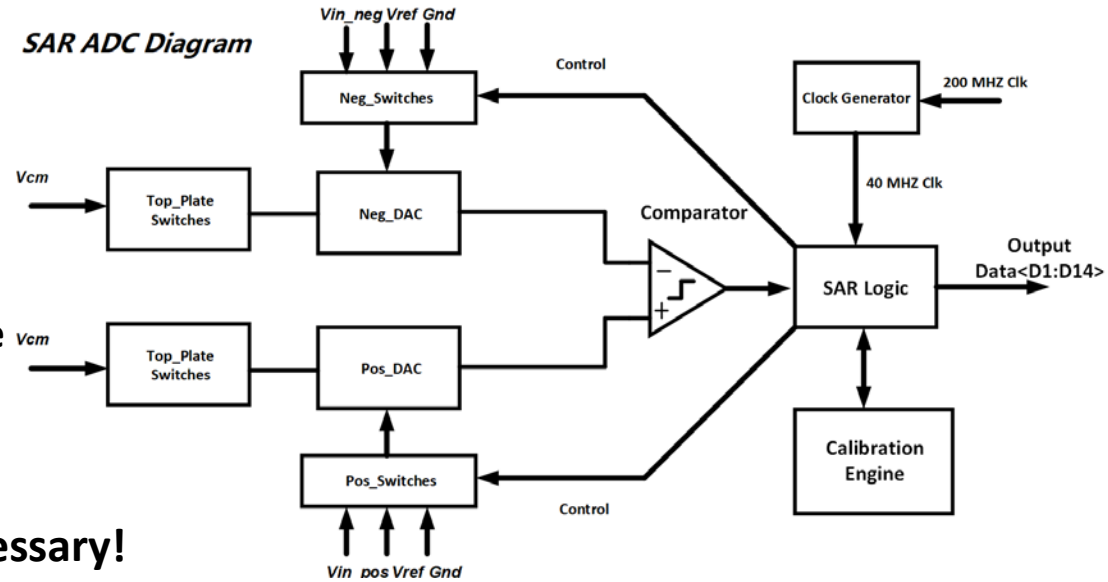
[Mei, Yethiraj, Vernon, Li_BNL LDRD]

- **Most blocks are passive components**
  -> less risk in cold environment

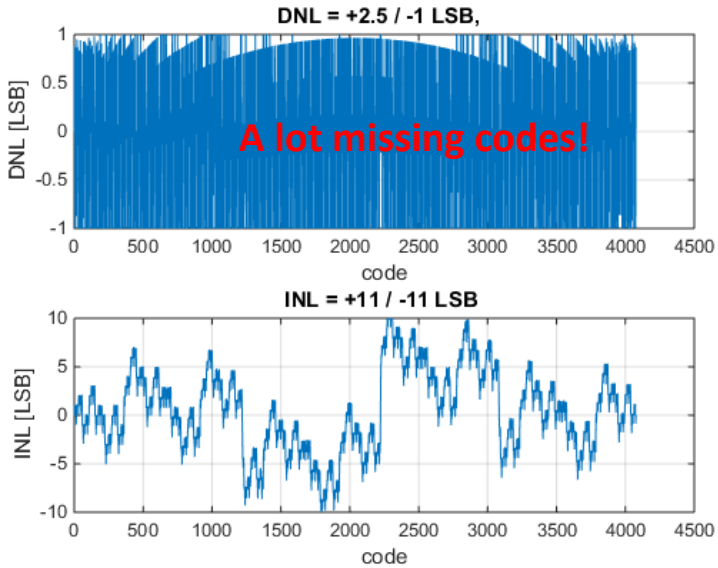
- **Major linearity error come from DAC capacitor mismatch**
  -> calibrated to obtain high resolution

- **MIM capacitor mismatch is NOT sensitive to temperature**

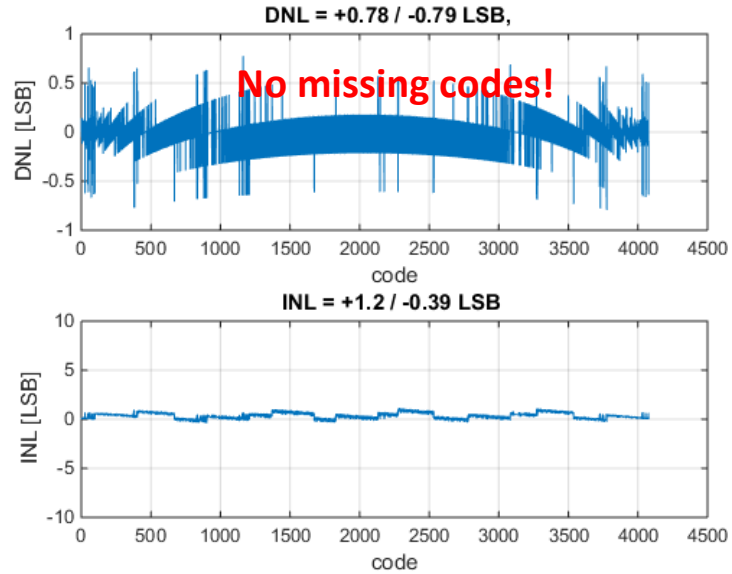
To achieve >10-bit resolution, DAC redundancy and calibration are necessary!



Without Calibration



With Calibration



LDO (Low Drop-Out) Regulator

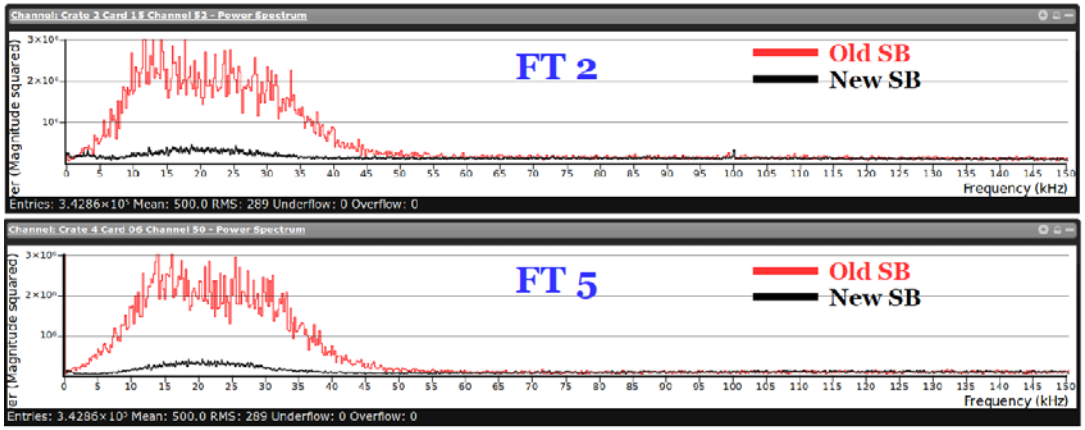
[Hou, Li_BNL LDRD]

- Commercial regulators are subject to trade-offs between noise and other general-purpose requirements which are not necessary for our FE-ASICs.
- Our goal: very low noise @ low power, optimized for LAr FE ASIC.

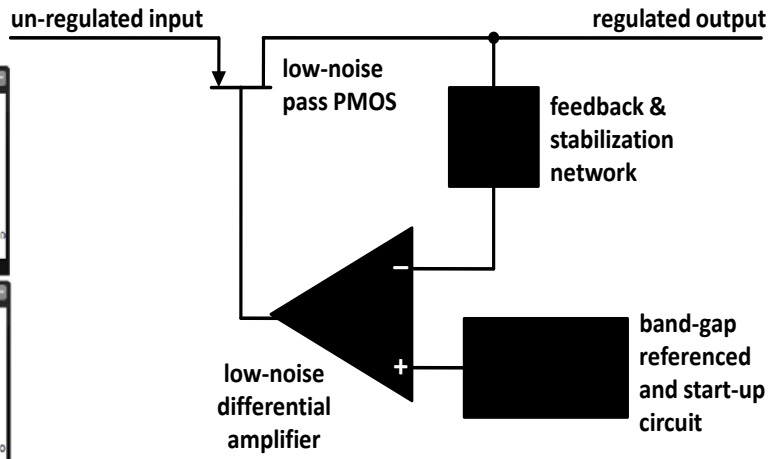
nV/sqrt(Hz) in LAr	@ 1 kHz (1/f)	>100kHz (white)
LAr ASIC Input PMOS	5	1.4
TPS78618 (uBooNE_ini)	200	50
ADP7159 (uBooNE_rev)	3	0.5

- **10k-30kHz noise observed in uBooNE, due to regulator noise amplified by the FE channel;**
- **Issue fixed by using lower noise regulator or heavier on–board filtering.**

uBooNE Service Board Test [Mooney_Aug2016]



- July 11th: tested service board with new LV filtering on FT 2 and with new voltage regulator on FT 5



Two-Dimensional, Pad Detector for Neutron Scattering

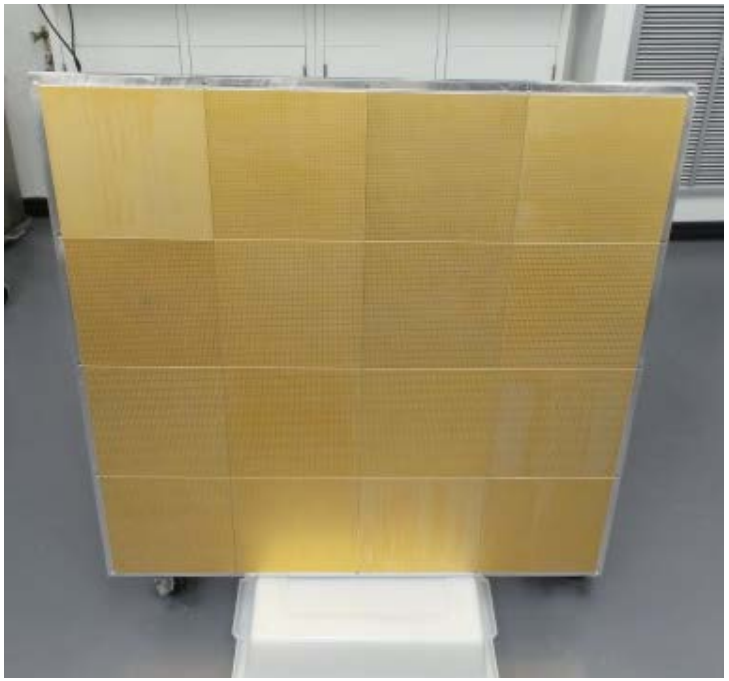
24 cm × 24 cm anode pad board, with 5mm × 5mm pads → 2304 pixels

$^3He + n \rightarrow {}^3H + p$ +764keV (~ 5 fC, or ~ 30k electrons)

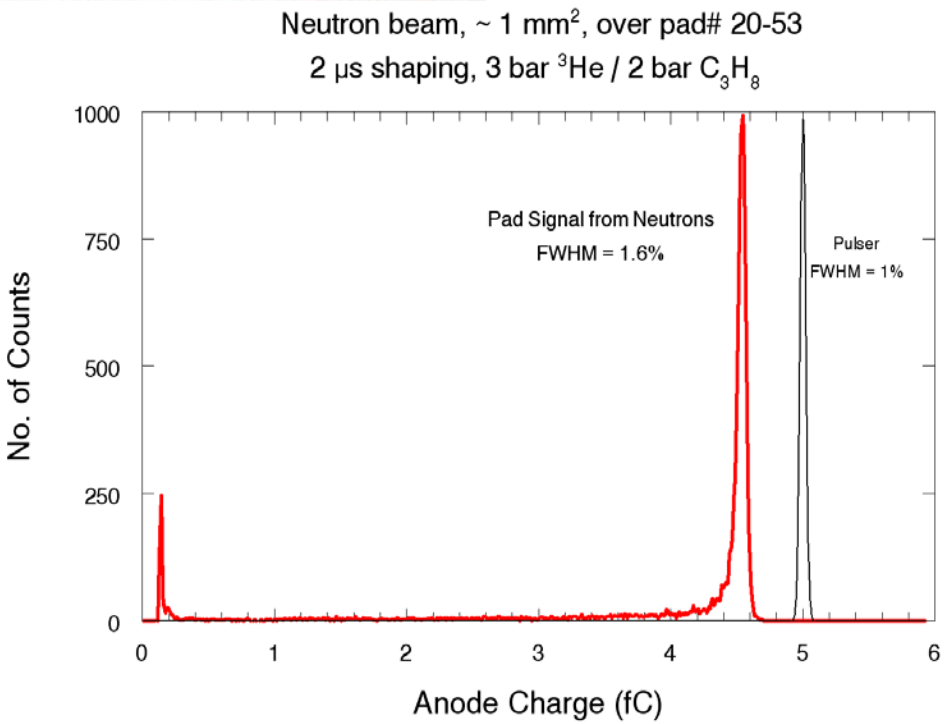
Array of 4 × 4 pad boards, comprising 37 k independent channels. Operation in ionization mode, i.e. unity gas gain, would not be not feasible without ASICs

SNS ASIC

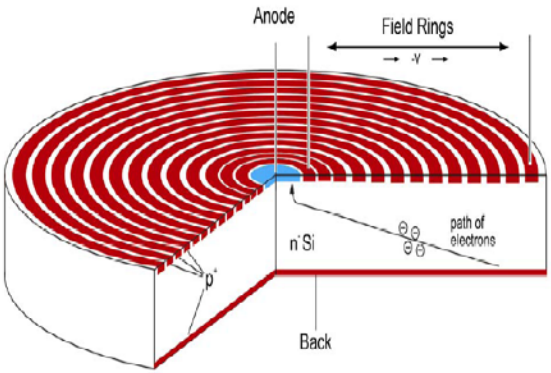
64 channel
2mW/ch



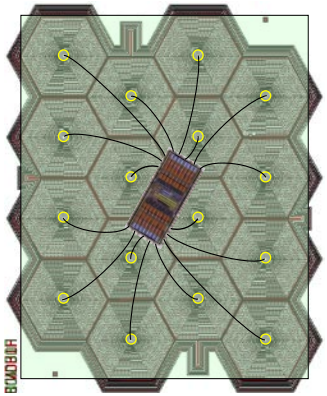
1 m × 1 m Detector for ANSTO



ASIC for High Resolution X-ray Spectrometers



[Rehak & Gatti _1983]



16 x 20mm² SDD pixels

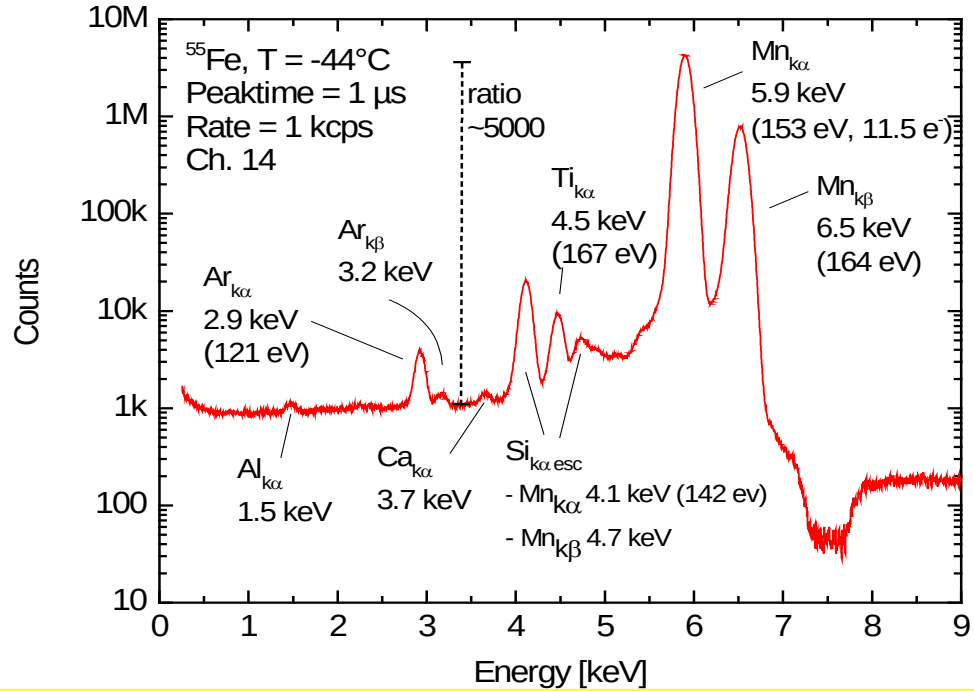
Improving Radiation Resistance:

- Radiation degradation due to leakage current of NMOS↑

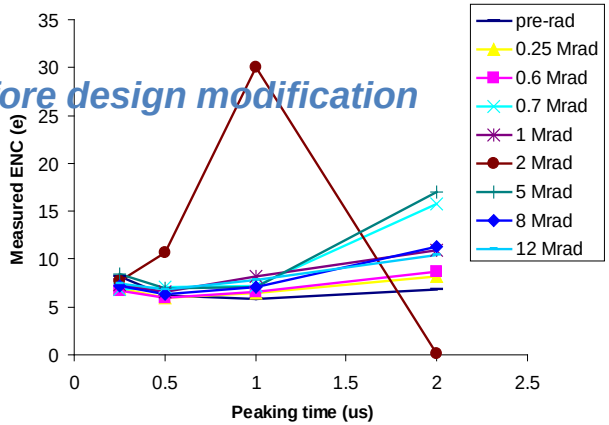
-ENC degradation: peak at around 2 Mrad

-Modified design to improve radiation resistance: replacing NMOS switch with PMOS switch; insert PMOS switch between NMOS current source and charge amp. input; increase device length; gate-enclosed layout.

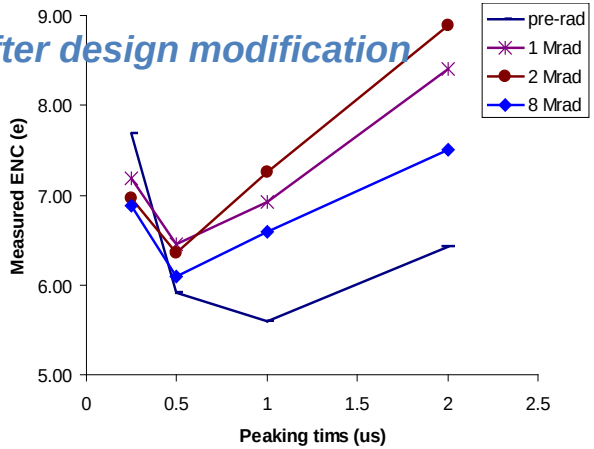
~11 e⁻ resolution (93 eV) with 20 mm² SDD pixel



ENC before design modification

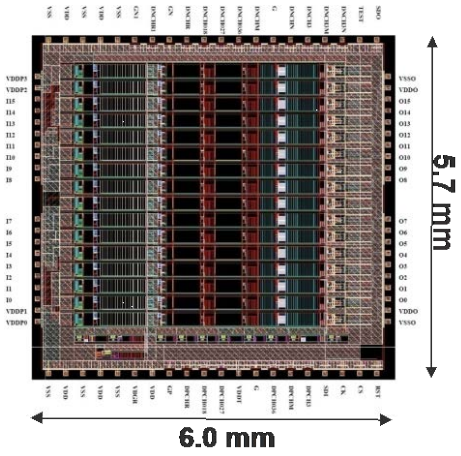


ENC after design modification

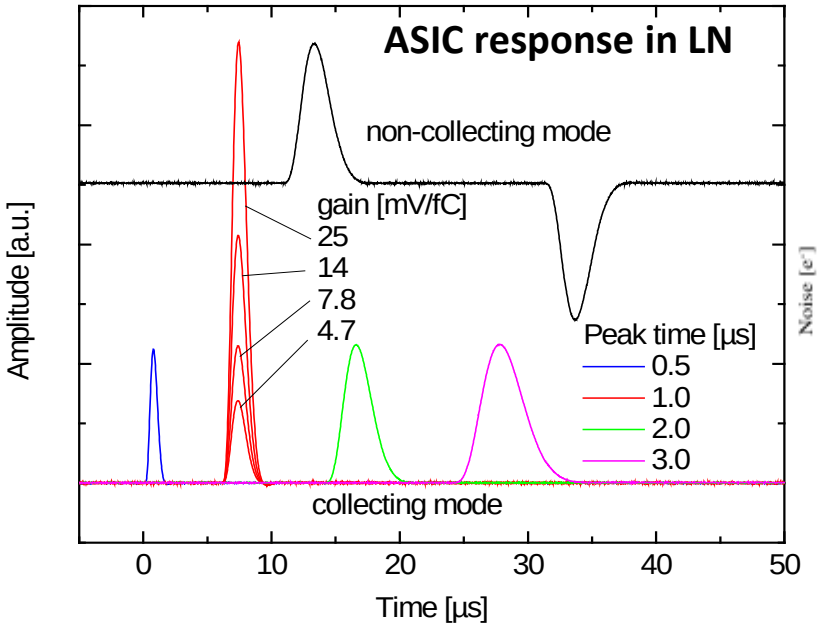


[S. Li, de Geronimo, et al., IEEE TNS 2013]

Cryogenic Analog Front-End ASIC

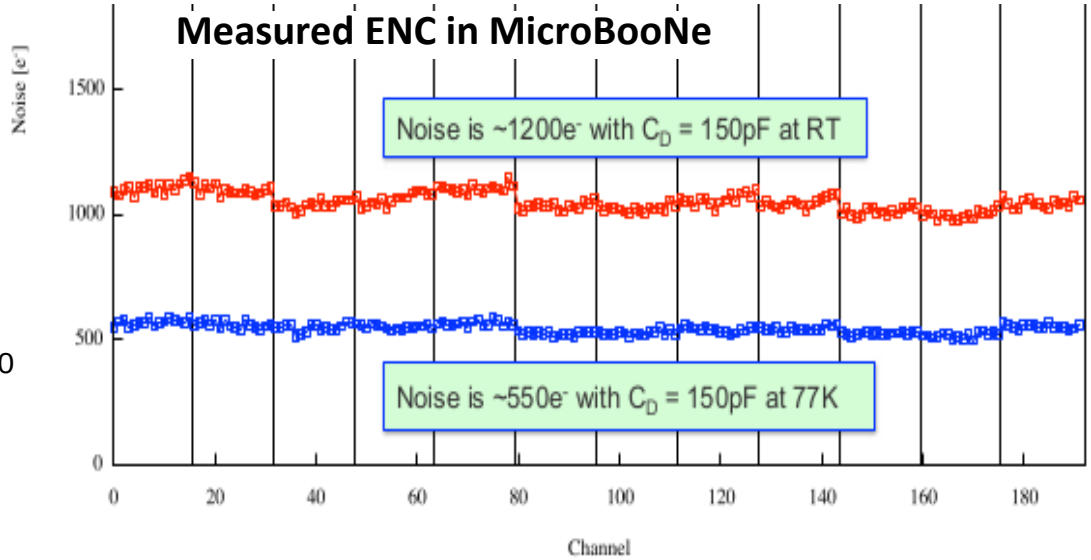


- 16 channels - charge amplifier, filter, buffer
- Adjustable gain: 4.7, 7.8, 14 and 25 mV/fC
- Adjustable filter time constant: 0.5, 1, 2, 3 µs
- Selectable collection/non-collection mode
- Selectable DC/AC (100 µs) coupling
- Band-gap referenced biasing
- Temperature sensor (~3 mV/ºC)
- 5.5 mW/channel (input MOSFET 3.6 mW)

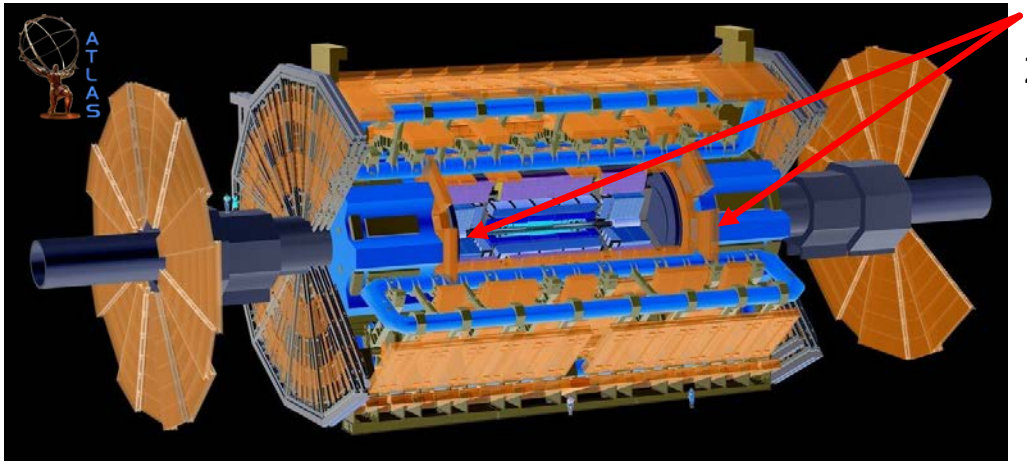


G. De Geronimo et al., IEEE TNS 58 2011

- Adopted in **MicroBooNE, DRIFT, Argontube, CAPTAIN, LArIAT, LBNF 35T, LAr1-ND, ICARUS (CERN),** candidate for **nEXO**

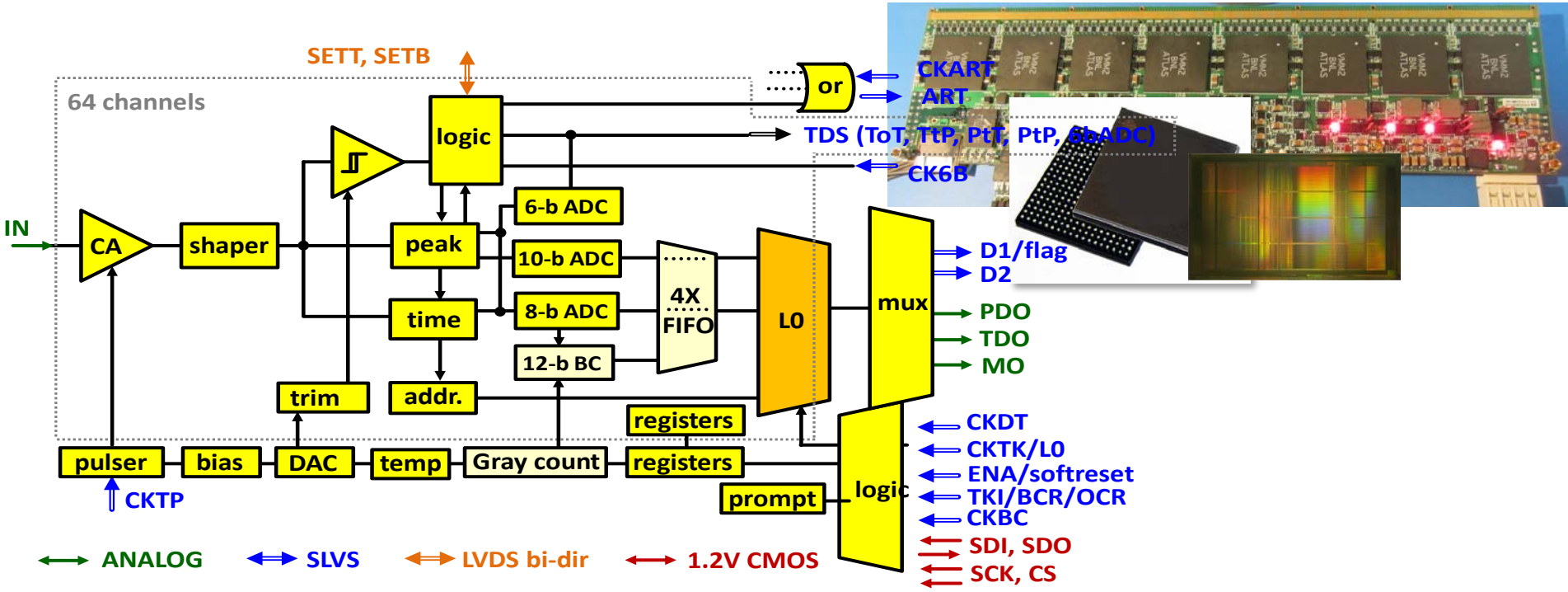


FE-SOC: ASIC for ATLAS Muon Spectrometer



New Small Wheels: 2.3M channels,
2pC @ < **1fC** rms, 100ns @ < **1ns** rms, 30pF-**2nF**

- **64 channels: low-noise amplification, peak, timing, discrimination, 3 ADCs, timestamp, FIFO, L0 handling**
- **real-time address, sub-hysteresis, direct outputs, fully digital interface**
- **CMOS 130nm, 13.5 mm x 8.4 mm,**
- **transistor count/ch.: > 100,000**



G. De Geronimo et al., IEEE TNS June 2013

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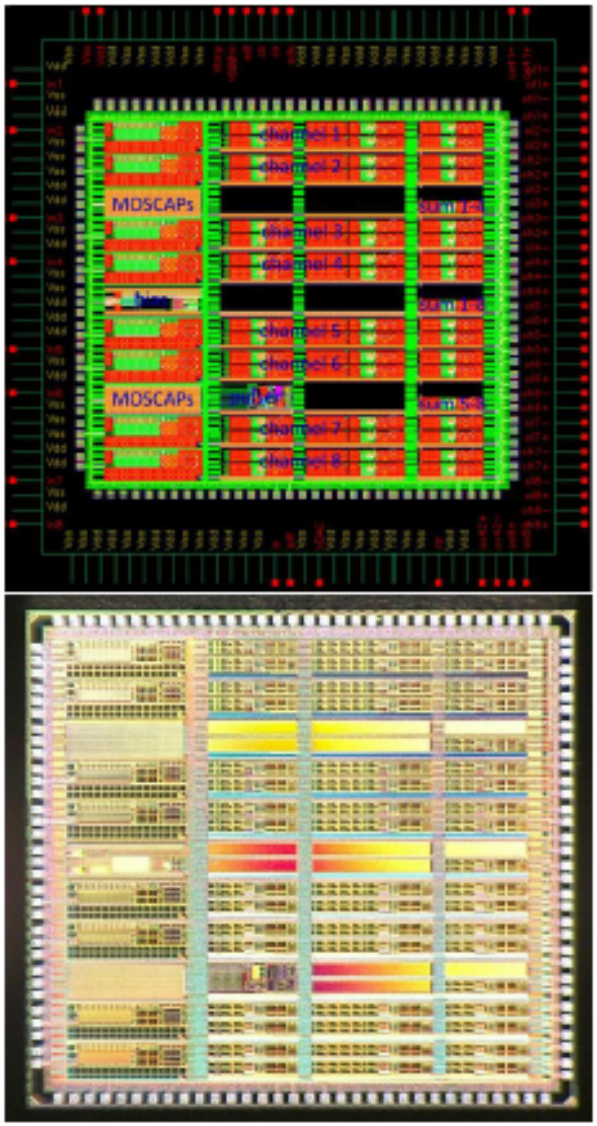
HLC1 FE ASIC



Outputs

- 16 x front-end channels
  - High gain, low gain output x 8 channels
  - Low-noise preamplifier
  - Programmable (25/50) internal termination
  - Differential output with ADC drivers
- 3 x summing channels
  - 2 x four-channel summing
  - 1 x eight-channel summing
  - Differential output with ADC drivers

Power Consumption

- 880 mW @ 1.2V => 733 mA

Configuration Interface

- 4 x 1.2V CMOS, SPI, 143 registers;

Package

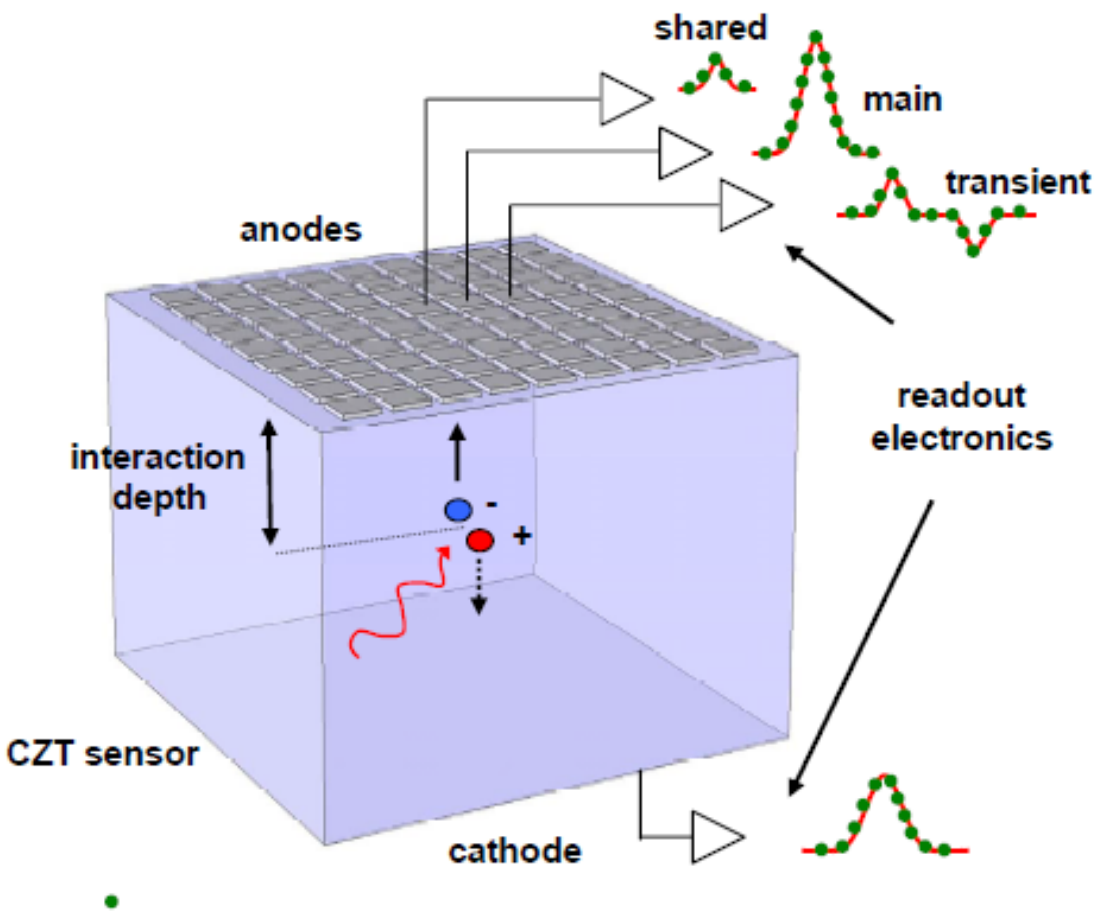
- 128 LQFP

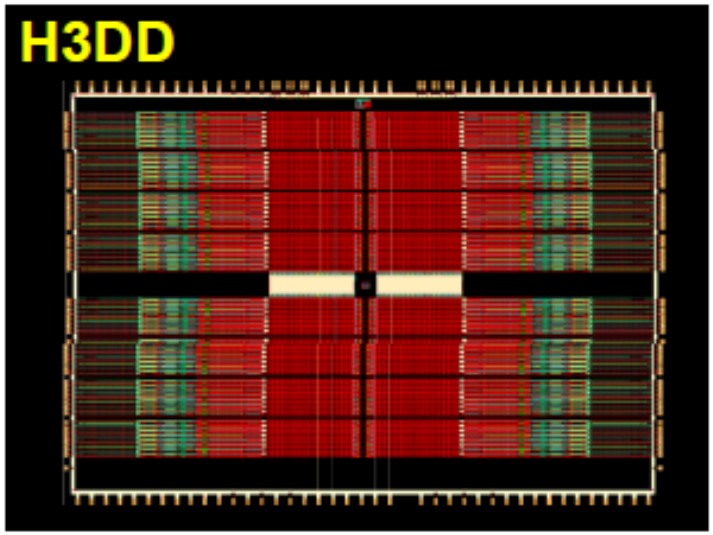
Other Features

- Pulse generator;
- Temperature sensor, biasing circuitry;
- 65 nm TSMC CMOS process;

[G. De Geronimo et al. IEEE NSS 2017]

Digital 3D PSD Technique - H3DD ASIC





- H3DD ASIC measures **whole waveform** on each signal
- Waveforms are analyzed with powerful signal processing techniques, thus achieving **higher resolution** *(Prof. Z. He)*

[G. De Geronimo_Sept2016]