eRD14: Photosensors and Electronics

Projects

- Photosensors in High Magnetic Fields (Y. Ilieva, C. Zorn)
- MCP-PMT/LAPPD (J. Xie, M. Chiu)
- Electronics (G. Varner, M. Contalbrigo, I. Mostafanezhad)

High-B Sensor Program
Commercial MCP-PMT Evaluation in High-B Fields

Y. Ilieva (USC), B. Moses (USC; T. Cao (UNH); C. Zorn (JLab),
J. McKisson (JLab); G. Kalicy (CUA); A. Lehmann (EU);
P. Nadel-Turonski (SBU); C. Schwarz (GSI), J. Schwiening (GSI);
Ch. Hyde (ODU)

Goals:

- Identify the limitations of operation of commercially-available MCP-PMTs in high B-fields: G(B, θ, φ), σ_t(B, θ, φ)
- Identify the most favorable orientation of sensors for high-B operations at EIC Example: tilt angle with respect to the local B-field; different sensor options
- Investigate suitable parameters for operations in high magnetic fields: HV

The High-B Facility is located at Jefferson Lab.

Commercial MCP-PMT Evaluation in High-B Fields: FY21

FY21 Planned Activities

- Full scan of 10-μm XP85122-S, HiCE Planacon: timing, gain, ion feedback (B, HV, θ, φ) **(on schedule, Summer 2021)**
- Full scan of a 6-μm Photek: timing, gain, ion feedback (B, HV, θ, φ). Size: 6x6 cm^2. Channels: 16x16. Pixel: 3 mm. A possible alternative to Planacon **(on schedule, Summer 2021)**

Progress in July 2020 - March 2021

- Purchase of a 32x32 XP85122-S, HiCE Planacon **(complete, delivered November).**
- Preparation of a signal readout of a few channels at JLab, Samtech connector or Condalign film, new preamp **(in progress)**
- On-loan agreement with Photek (6 μm) – negotiated for Summer 2021
- USC Magellan scholarship awarded to Benjamin Moses to work on High B at JLab (student salary for 4 weeks and transportation)

Commercial MCP-PMT Evaluation in High-B Fields

Future activities

- Complete the scan of 10-μm XP85122-S, HiCE Planacon: timing and gain for various $HV_{Cathode-MCP1}$, $HV_{MCP1-MCP2}$, $HV_{MCP2-Anode}$ (1 run)
- Procure one 6-μm Photek and complete the scan: timing and gain for various $HV_{Cathode-MCP1}$, $HV_{MCP1-MCP2}$, $HV_{MCP2-Anode}$ (1 - 2 runs)
- Full-area gain, timing, and uniformity characterization of MCP PMTs for DIRC prototype with Uni-Hawaii electronics (1 - 2 runs)
- B-field scan of timing, gain, and ion-feedback of Gen-III LAPPD (2 runs)

MCP-PMT/LAPPD^{TM}

ANL: Whitney Armstrong, Sylvester Joosten, Jihee Kim, Chao Peng, Lei Xia, **Junqi Xie**

BNL: Bob Azmoun, **Mickey Chiu**, Alexander Kiselev, Craig Woody

Incom: Michael Foley, **Michael Minot**, Mark Popecki

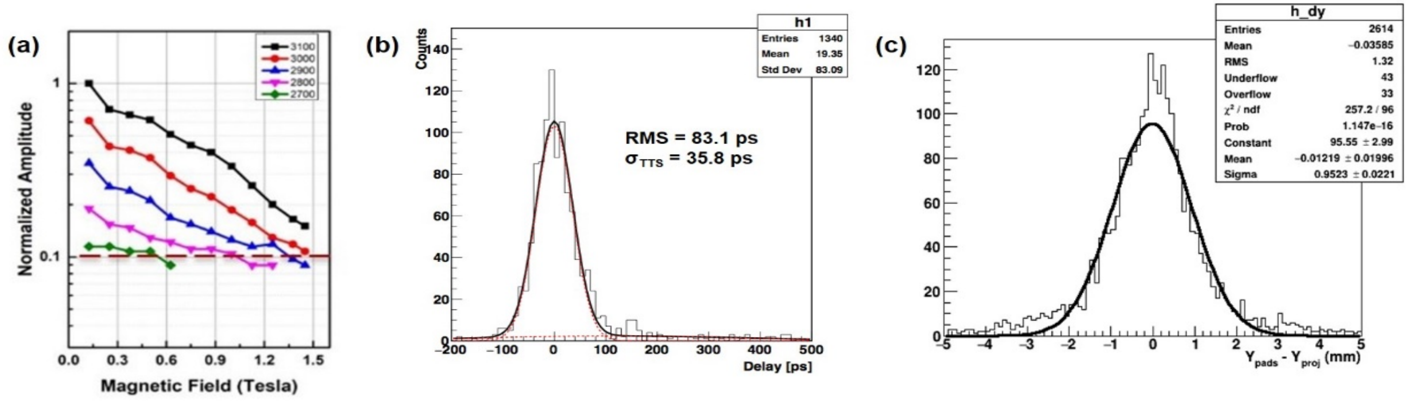
Goal

Adapt LAPPD^{TM} to the EIC requirements: Highly pixelated LAPPD^{TM} working at 2~3 Tesla for mRICH, dRICH, and DIRC, as well as TOF applications.

Argonne MCP-PMT: Current status

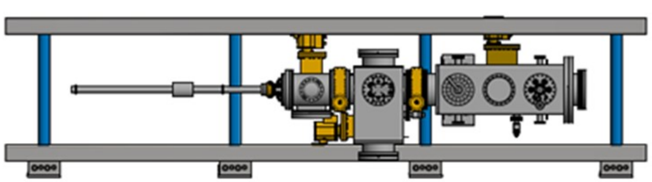
Demonstrated applicable performance for EIC Cherenkov detector sub-systems:

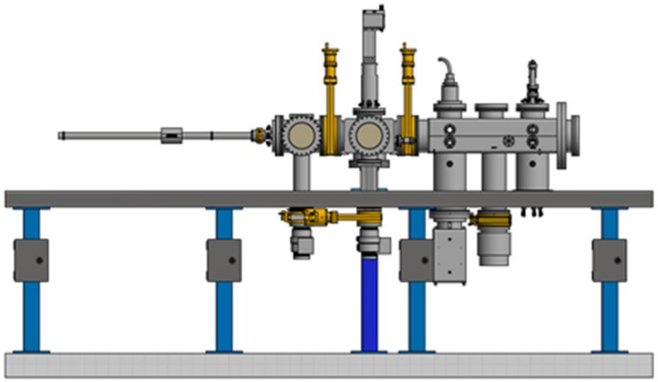
- Magnetic field tolerance > 1.5 Tesla
- RMS timing resolution < 100 ps
- Position resolution < 1 mm with 3mm x 3mm pixel size



Transition to fabrication of 10x10 cm^2 MCP-PMT prototypes

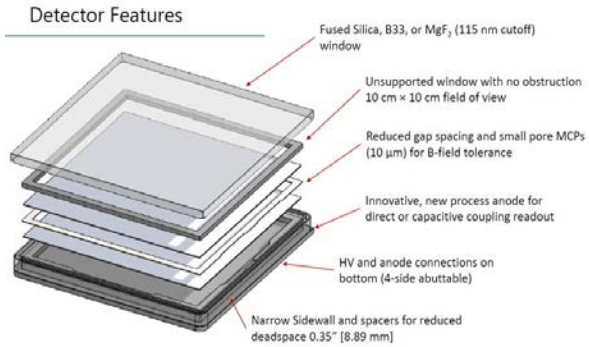
- Fully integrated pixelated and magnetic field tolerant MCP-PMT design
- Upgraded fabrication facility with full oven baking for device fabrication
- MCP-PMT size of 10x10 cm^2 applicable for both R&D and prototype validation





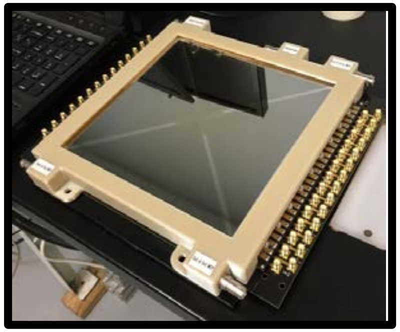
Incom Pixelated Gen-II and -III LAPPD Status

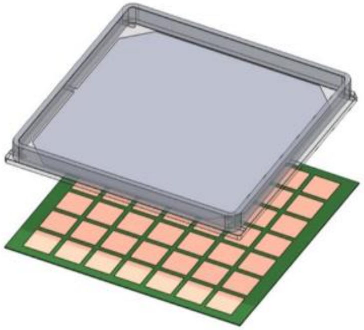
SBIR phase I "**Large Area Multi-Anode MCP-PMT for High Rate Applications**" was awarded.

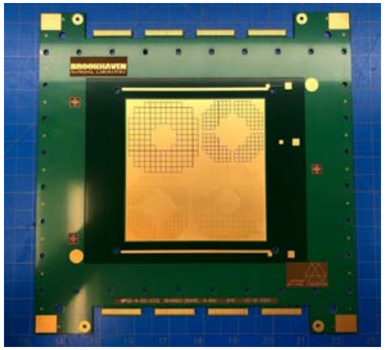


- ANL 10 μm ALD-MCP-PMTs R&D results were integrated in the HRPPD design. The sensor is read out using LTCC ceramic anode (hpDIRC application).
- First HRPPD delivery of summer 2021.

SBIR phase I "**Application Specific High Fluence Anode Design**" was awarded.







- Joint Incom, Nalu, BNL and ANL effort to explore Gen-II pixelated LAPPD and its readout for EIC RICH sub-systems
- One Gen-II LAPPD

Proposed FTBF Experiment in Spring 2021

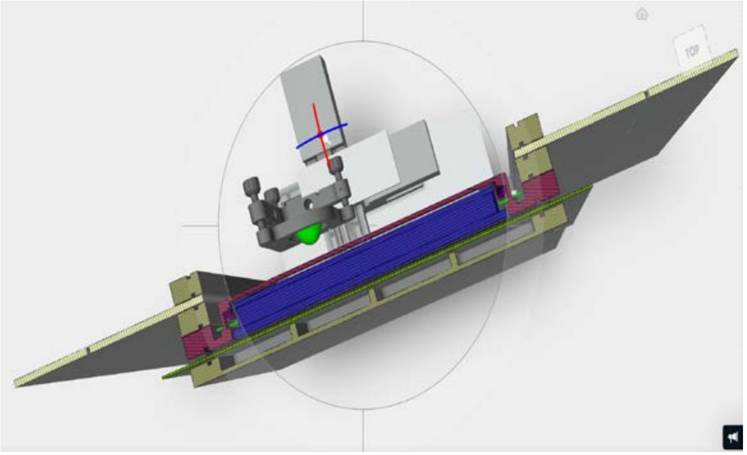
Originally planned in Mar, now delayed to May

Available devices for EIC-PID

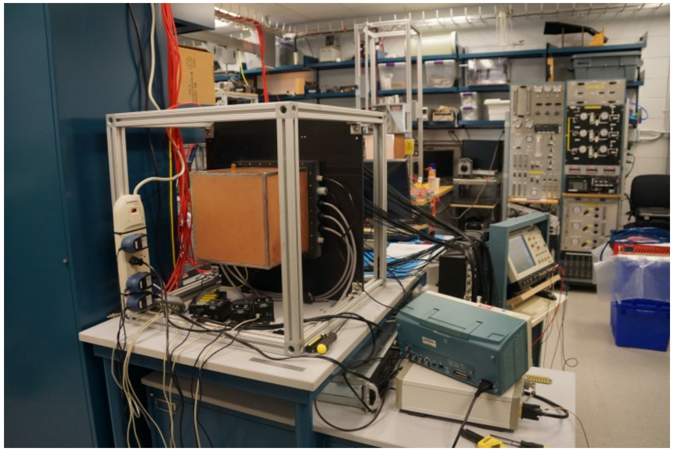
- Gen-II LAPPDs on loan to EIC consortium since Dec 2020.
- Two ANL 10um MCP-PMTs

Proposed beam-line tests (work with mRICH and eRD6 MPGD groups)

- In beam performance validation of Gen II LAPPDs and ANL MCP-PMTs
- mRICH-LAPPD-ToF experiment for combined RICH and TOF test with LAPPD, mRICH module has been received and setup at BNL.



LAPPD setup in beam CAD model



Test stand setup in lab

Future activities and projection

FY2021

- Complete **beamline validation** of Gen-II LAPPD and ANL 10 μm MCP-PMTs with simple pixel readout
- Complete **mRICH-LAPPD-ToF experiment** with LAPPD
- **Magnetic field test** of one Gen-II LAPPD and one Gen-III HRPPD

Future projections

FY2022

- **Fabrication** of a 10x10 cm MCP-PMT prototype for validation
- **Evaluation** of LAPPD and HRPPD in bench and magnetic field tests
- **Integration** of Gen-II LAPPD and 10x10 cm MCP-PMT with external pixelated anode and Hawaii HDSoC electronics

FY2023 and beyond

- **Further improvement** of Gen-II LAPPD and 10x10 cm MCP-PMT for fine pixel size readout and signal pickup
- **Beamline evaluation** of Cherenkov detector sub-systems with LAPPD and 10x10 cm MCP-PMTs

Readout Electronics
for eRD14 Prototypes (and beyond)

Marco Contalbrigo – INFN Ferrara

Isar Mostafanezhad - Nalu Scientific

Gary Varner – University of Hawaii

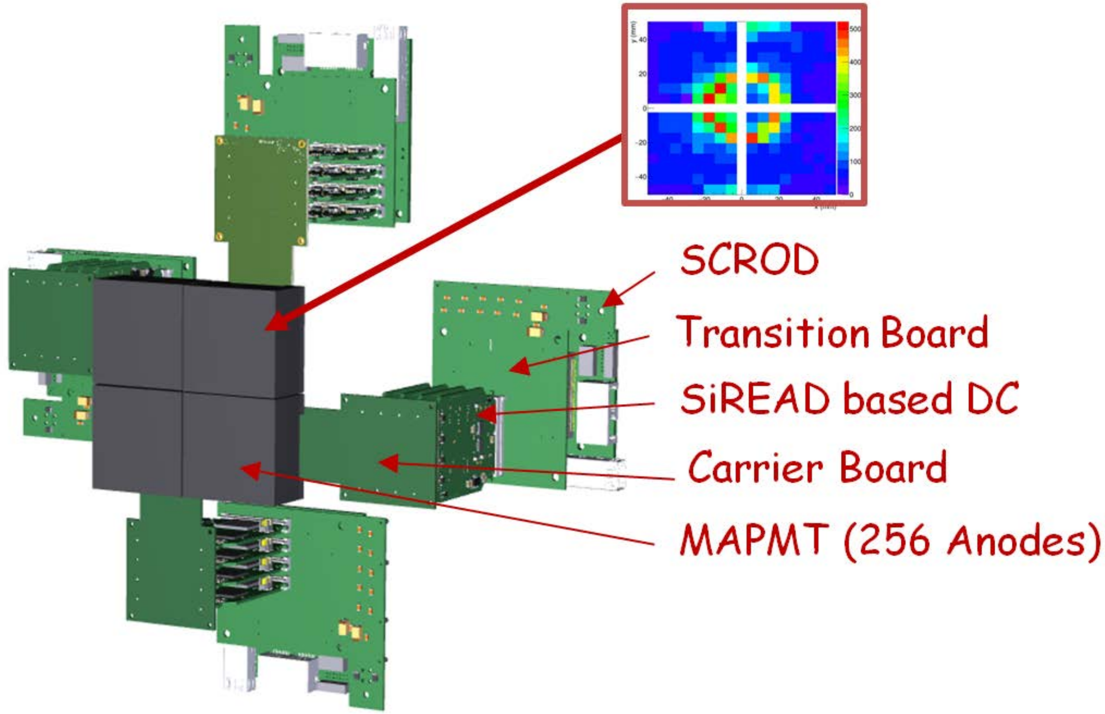
Goals

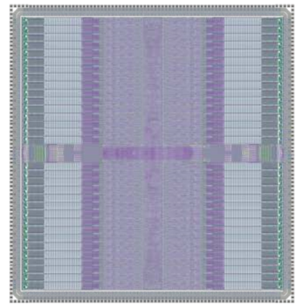
- Develop an integrated suite of readout electronics for the different photo-sensors used for all the Cherenkov detectors and prototypes
- Provide a reference readout system for prototypes performance assessment
- Develop a generic DAQ system compatible with the eRD14 needs
- Test applications with various sensors (including SiPMs)

Readout Electronics for eRD14 Prototypes

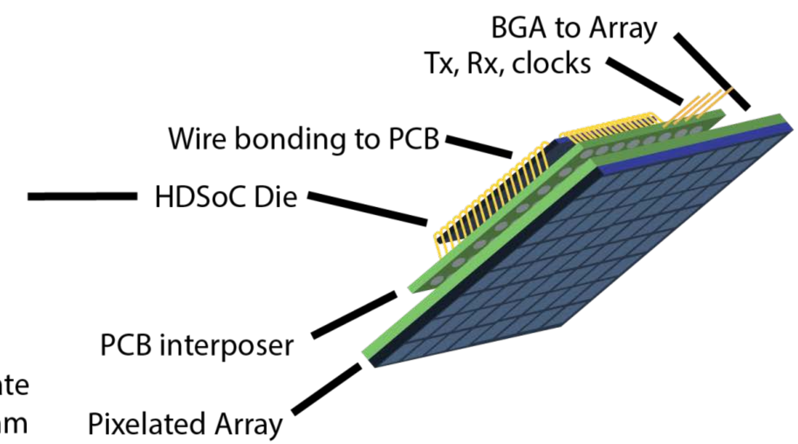
Ongoing Activities

- Development of SiREAD based readout firmware to operate with the SCROD FPGA
- Second generation firmware to improve data throughput for front-end to back-end communication, including introducing triggerless readout
- Transition from the SiREAD (32-channel) chip to HDSoC (32, 64 channel)
- Evaluation of alternative readout architectures based upon ToT/TDC architectures (separate slide)





Nalu Scientific
HDSoC V1 64 channel estimate
64 channel = 7.2 mm x 7.4 mm



Readout Electronics: ToT architecture alternatives @ INFN

Ongoing Activities :

Development of a ToT readout based on
ALCOR (F/E) + ARCADIA (DAQ)

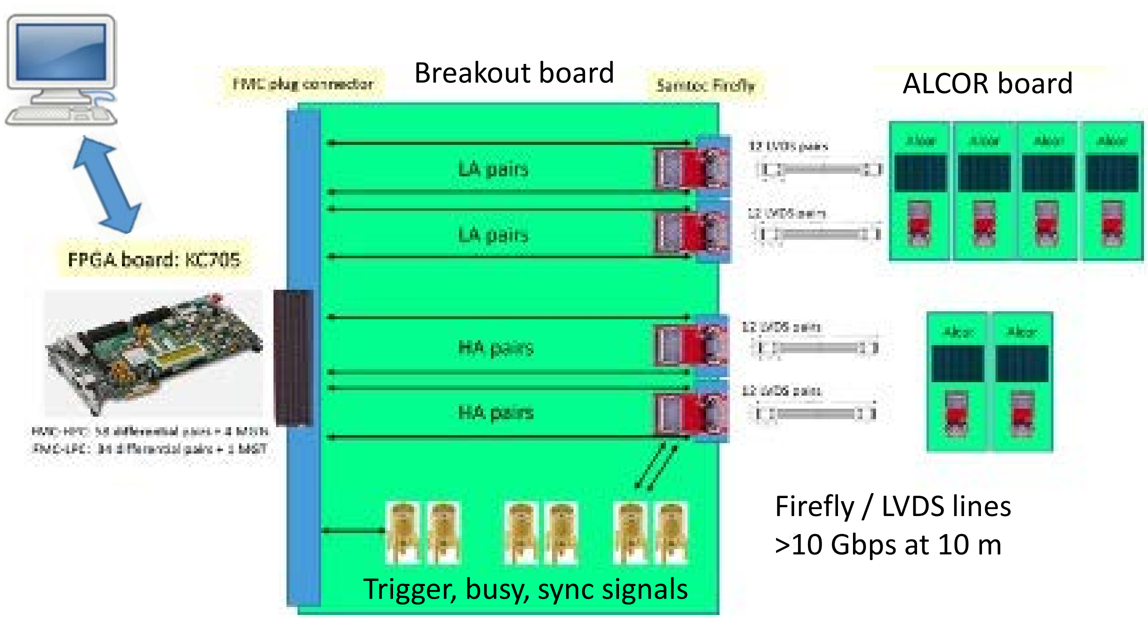
- 500 kHz per channel
- 50 ps time binning

Chip under validation with a dedicated test board

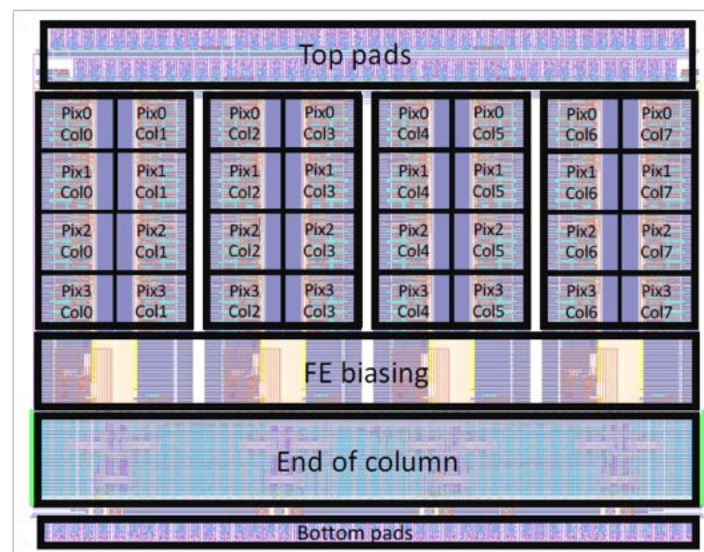
Design of a readout chain dedicated to dRICH / SiPM

Development of a portable high-rate DAQ & firmware

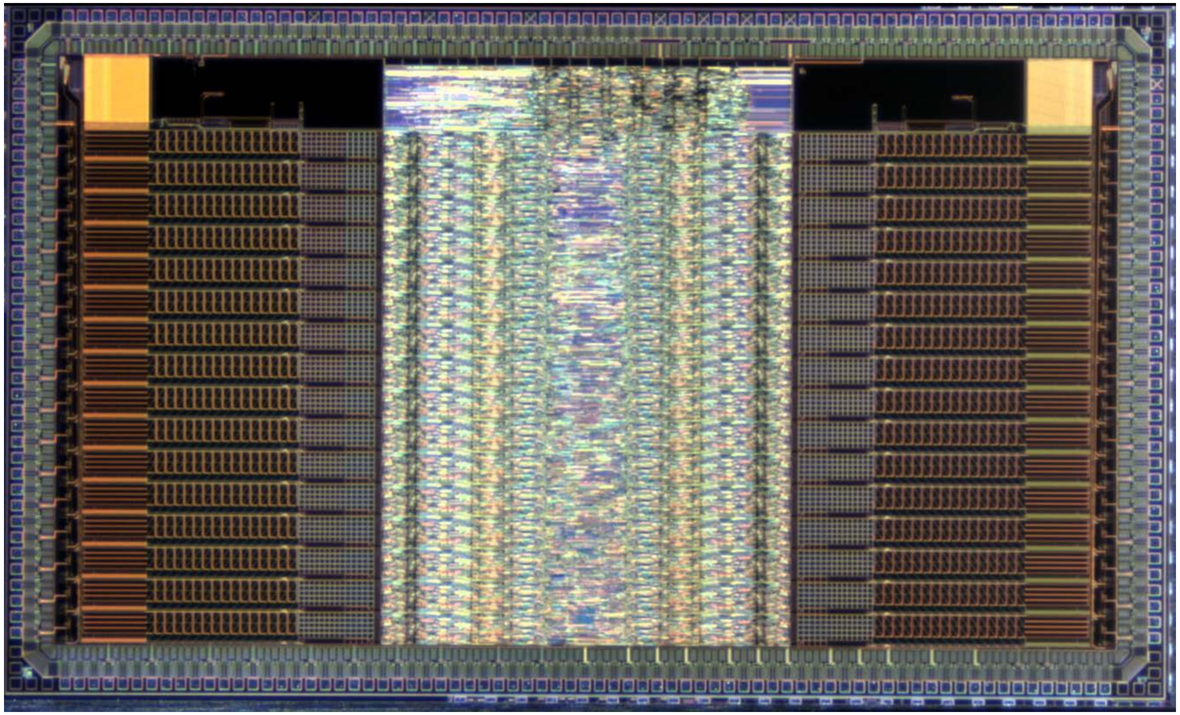
Test station



ALCOR: flexible gain and discrimination
2x TI amplifier per channel (gain)
4x TDC per channel (edge/rate)



Readout Electronics



Future activities

- Complete evaluation of Si-READ ASIC based readout
- Upgrade to the (32-channel) HDSoC ASIC when ready in May/June 2021
- Build 1k channel integrated readout demonstrator mRICH, using 64-channel HDSoC (final prototype system, will permit WBS costing)
- Explore ToT alternative in parallel at INFN
- Comparison summary: performance, power, cost, availability, integration

Backup Slides:

MCP-PMT/LAPPD^{TM}

ANL: Whitney Armstrong, Sylvester Joosten, Jihee Kim, Chao Peng, Lei Xia, **Junqi Xie**

BNL: Bob Azmoun, **Mickey Chiu**, Alexander Kiselev, Craig Woody

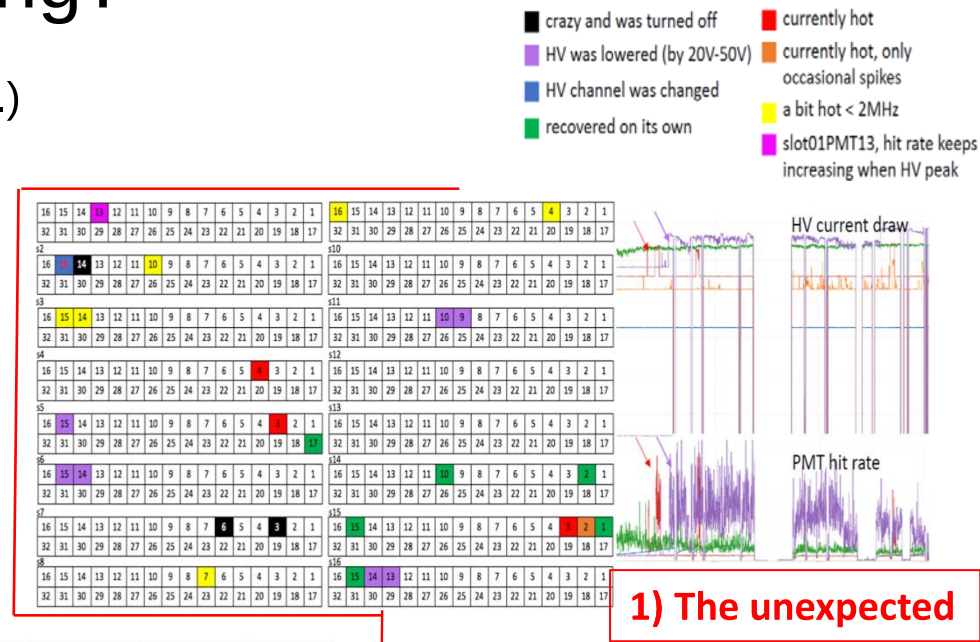
Incom: Michael Foley, **Michael Minot**, Mark Popecki

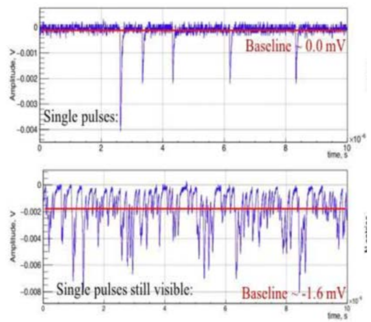
FY21 Report

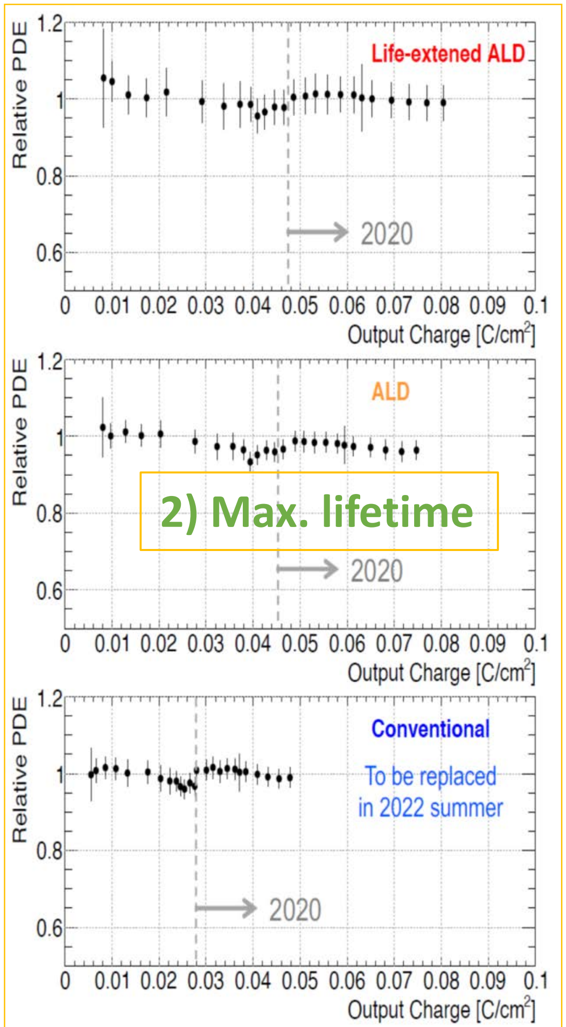
- **Fabrication of Argonne MCP-PMT** with integrated pixelated readout and magnetic field tolerant design
- **Full engagement of Incom** to develop pixelated Gen-II LAPPD and Gen-III HRPPD for EIC-PID Cherenkov needs
- Obtain a loan of Incom 20x20 cm^2 pixelated LAPPD for bench test
- **Preparation of Fermilab beamline test** with MCP-PMT/LAPPD devices and mRICH module

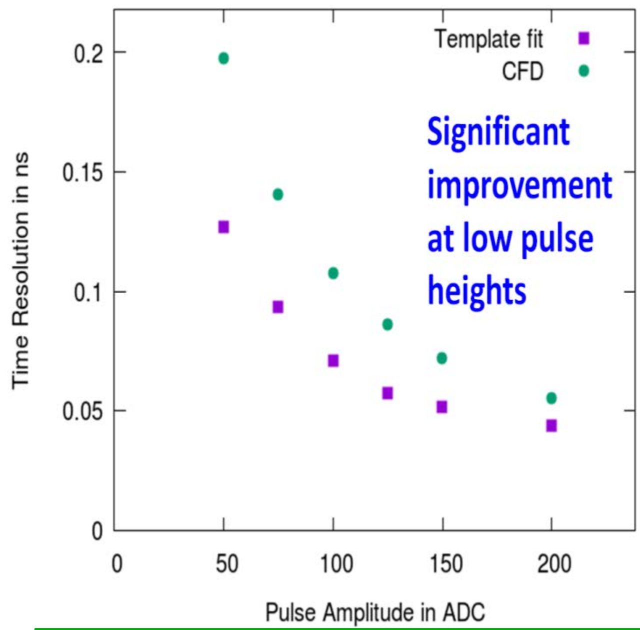
Why waveform sampling?

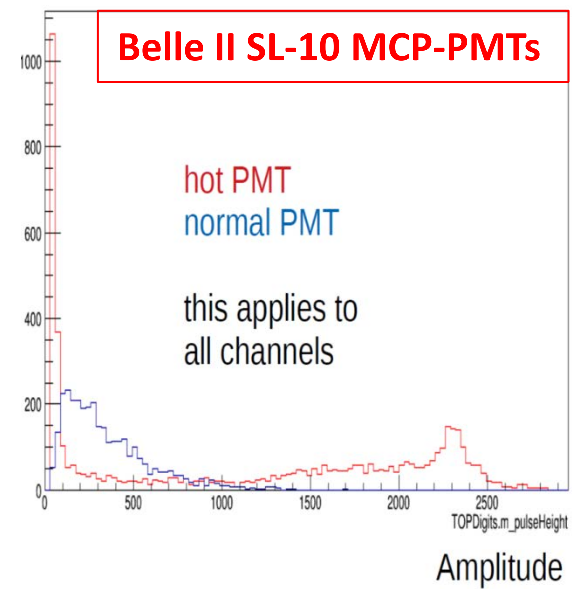
- CF: Amp+Disc+TDC (often TOT for ampl. Est.)
- 3 reasons (besides cost)





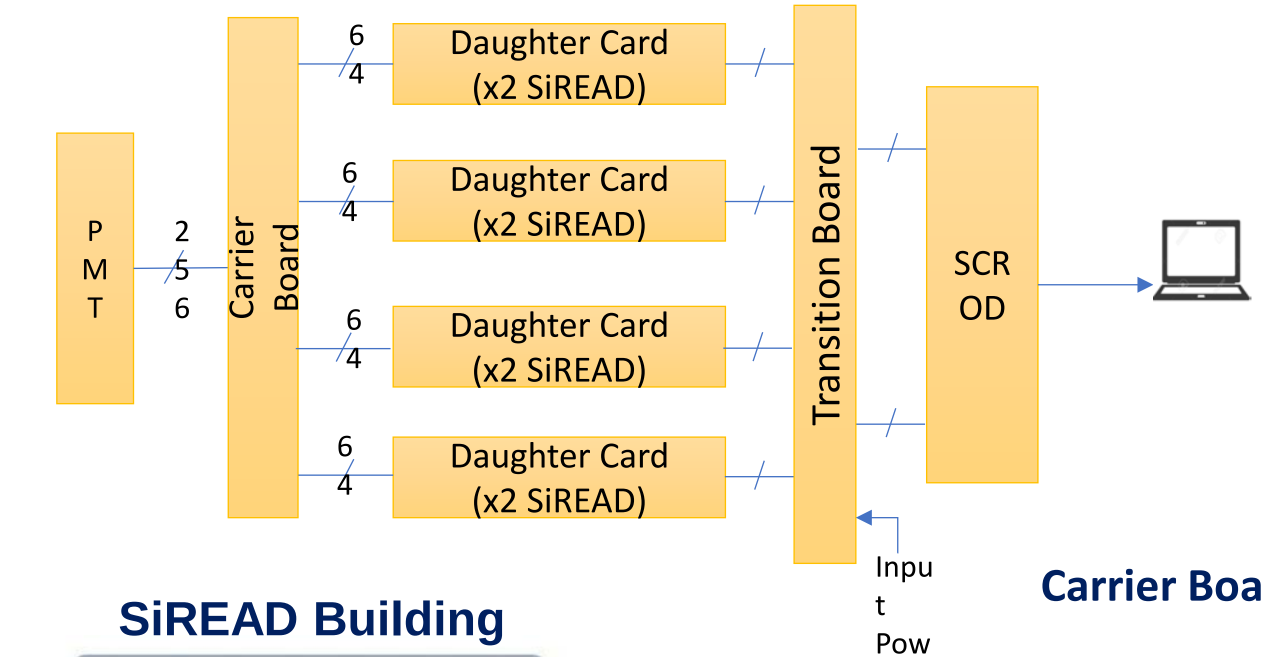




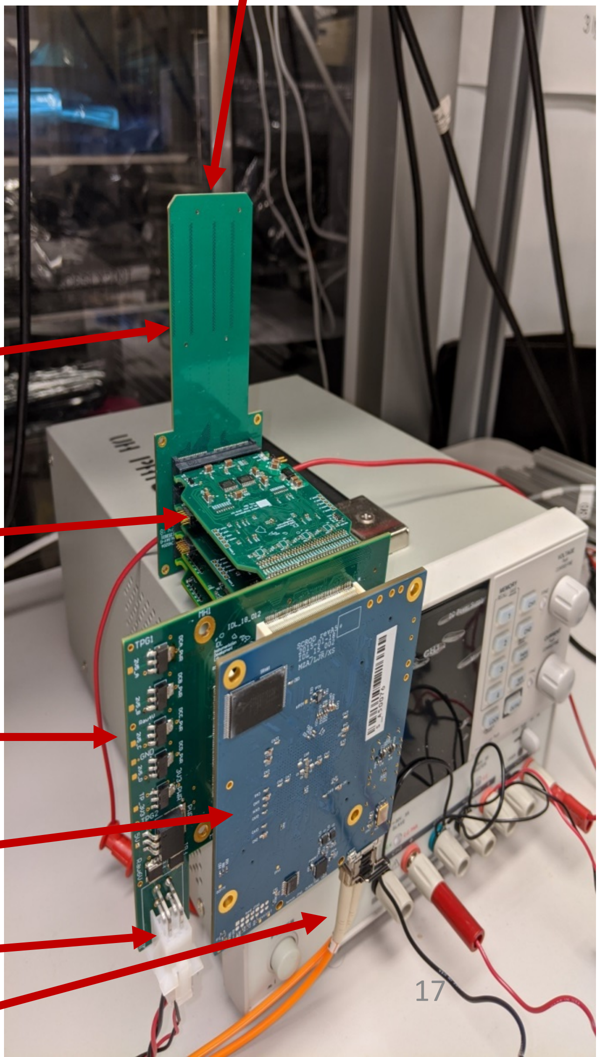


3) Optimizing (timing) performance

Readout Electronics overview



PMT mounts on the other side of the Carrier Board



Carrier Board

SiREAD DCs x4

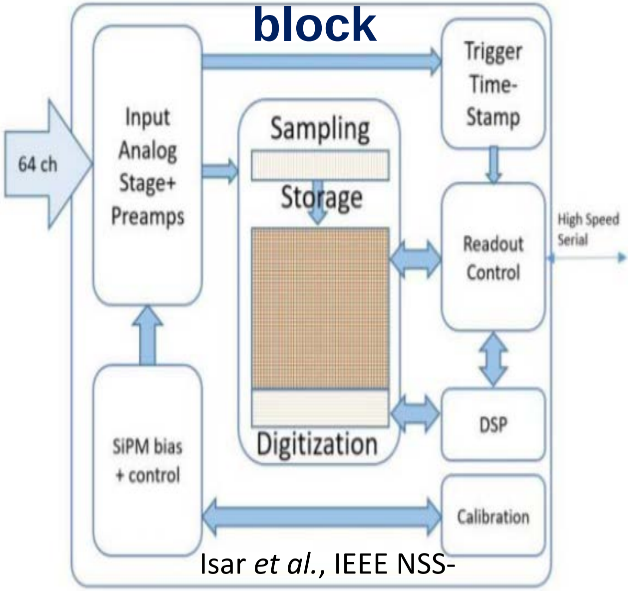
Transition Board

SCROD

Input power

optical gigabit transceiver

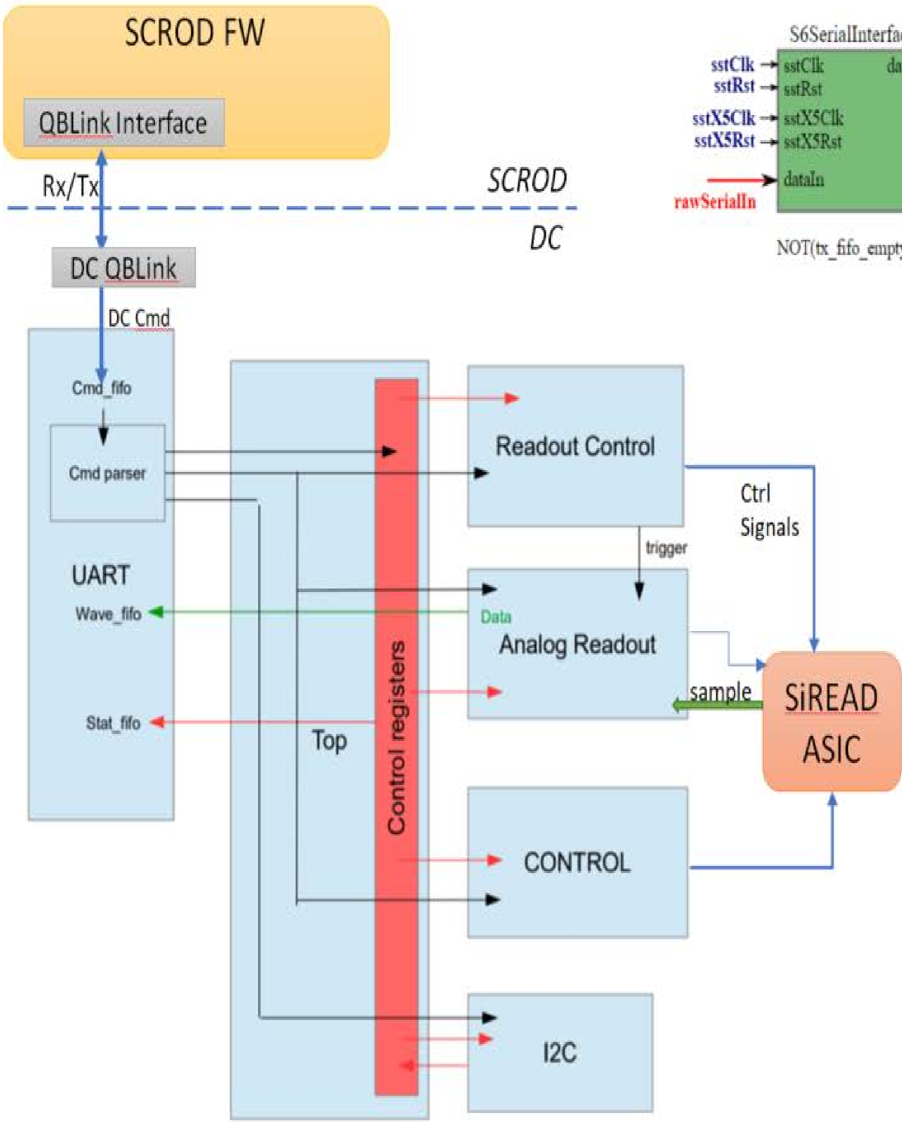
SiREAD Building block



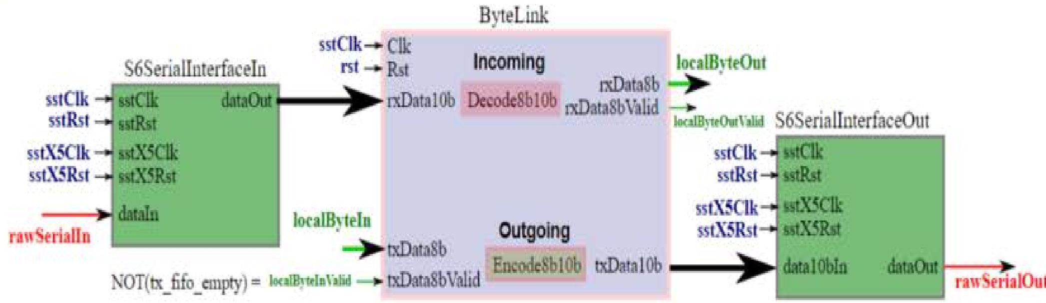
Isar *et al.*, IEEE NSS-2018

SiREAD Parameter	Specifications
Channels	32
Sampling rate	1 GSa/s
Storage samples/ch	4096
Est. Analog BW	0.7-1.1 GHz
RMS voltage noise	1.3 mV
Signal voltage range	2.1 V
ADC on chip	12 bits
Readout	Serial LVDS
Power consumption	20-40 mW/ch

SiREAD DC Firmware



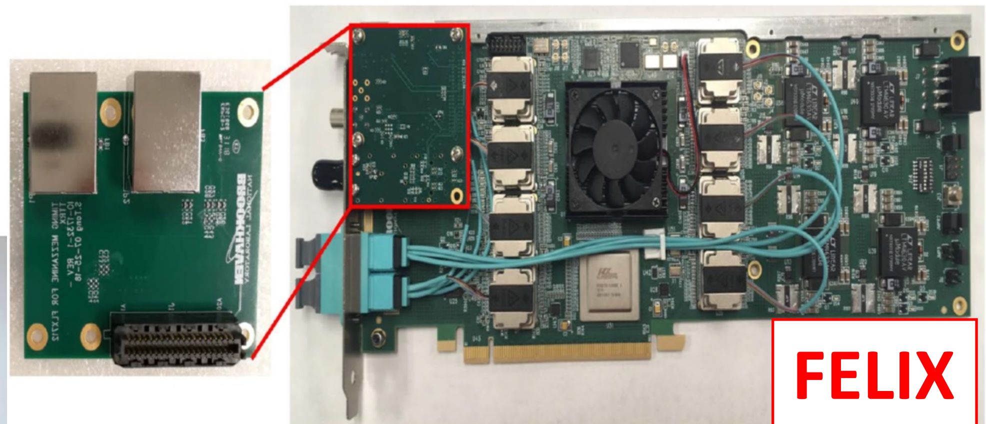
Quad Byte line (QBlink)

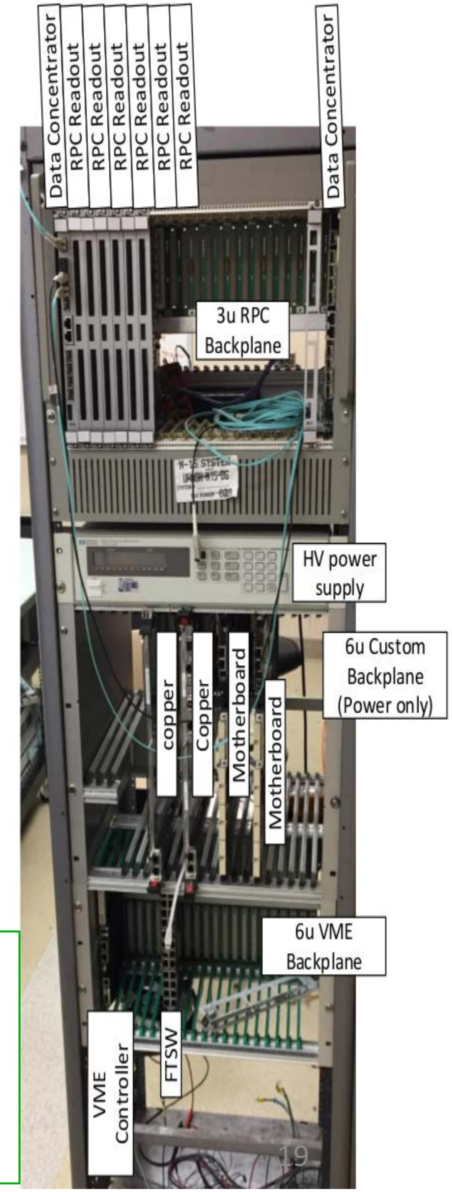


- Communication links between the SCROD and DCs is maintained using **QBLink**
- **Readout Control:** starts and stops acquisitions and handles triggers
- **Analog Readout:** handles the control of the SiREAD ASIC including write/read location and the actual readout
- **CONTROL:** writes the analog register

Backend Control/Readout: Belle II DAQ upgrade

- Current: JLAB and Belle2link readout as baseline
- Experience with Belle-II DAQ upgrade





Hawaii
Belle II KLM+TOP
DAQ upgrade
Test bench