

## EIC Detector R&D Progress Report

**Project ID:** eRD18

**Project Name:** Precision Central Silicon Tracking & Vertexing for the EIC

**Period Reported:** October 1 to December 31, 2018

**Project Leader:** Peter G. Jones

**Contact Person:** Peter G. Jones

### **Project Members:**

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### **Abstract**

We propose to develop a detailed concept for a central silicon pixel detector for an Electron-Ion Collider at BNL or JLab exploring the advantages of depleted MAPS (DMAPS) in HV-/HR-CMOS technologies to achieve improved spatial resolution and timing capability over traditional MAPS. The sensor development will exploit the Birmingham Instrumentation Laboratory for Particle Physics and Applications. An accompanying simulation study will optimise the basic layout, location and sensor/pixel dimensions to find the best achievable momentum resolution and vertex reconstruction resolution. This initial design study will allow future full-detector simulations to explore precision measurements of heavy flavour processes and scattered electrons at high  $Q^2$ .

## **1 Past**

### **1.1 What was planned for this period?**

Our proposed programme of work for FY19 was divided into two work packages: WP1 on sensor development and WP2 on detector layout investigations.

For this period, the plan for WP1 was to continue the characterisation of the modified TowerJazz (TJ) 180 nm CMOS process with two new prototypes of the TJ investigator chip. As reported in July, we have identified this technology as the most suitable for an EIC DMAPS sensor. It is the only available technology that can achieve a fully depleted sensor using a small collection electrode, which results in a small pixel size, low noise, and low power. In addition to the technology investigation aspect of this WP, we also proposed to work with chip designers at the Rutherford Appleton Laboratory (RAL) to explore different pixel designs and readout architectures to arrive at an EIC specific DMAPS sensor. This design work starts from an initial set of specifications that we presented in our previous report and aims to optimise pixel size

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and power consumption taking into consideration constraints coming from the detector simulations in WP2. The design work will provide feedback to the EIC DMAPS sensor specifications and the detector layout investigations.

The aim of WP2 is to optimise the detector layout of the central barrel through simulation studies of charmed hadron decays and high  $Q^2$  scattered electrons. This work is being carried out in collaboration with eRD16 who focus primarily on the forward tracking regions. In our report and presentation to the Committee in July, we showed the results of initial studies on momentum resolution and impact parameter resolution for pions in a 4- or 5-layer silicon tracker and compact TPC modelled in EicRoot. Results were presented for pixel sizes ranging from  $20 \times 20 \mu\text{m}^2$  to  $40 \times 40 \mu\text{m}^2$ . The momentum resolution was shown to be rather insensitive to the choice of pixel size at low transverse momentum ( $p_T < 5 \text{ GeV}/c$ ), whereas the impact parameter (pointing) resolution clearly favours smaller pixels. The inclusion of a thicker (1.6%  $X/X_0$ ) outer timing layer was not found to degrade the tracking and vertexing performance of the central tracker. The plan for this period was to consider the integration of the forward disks, particularly in the pseudorapidity interval  $1 < |\eta| < 2$  where the acceptance of the disks overlaps with that of the central barrel.

### 1.2 What was achieved?

#### WP1 – Sensor development

In the past 5 months, work on WP1 has progressed both on the technology characterisation and on the DMAPS design studies. In addition to the TJ investigator 1 chip (TJ1), we now have access to two new versions of the chip: the TJ investigator 1 bis (TJ1b) and TJ investigator 2 (TJ2). The design of the TJ1b and TJ2 is largely based on the previous version, each having over 100 matrices of  $10 \times 10$  pixels with various sizes of collection electrode and spacing between the collection electrode and the deep p-well which will contain the electronics. The new versions incorporate a few additional features. In both the TJ1b and TJ2, the p-substrate and the p-well for the electronics can be biased separately to allow for higher substrate bias and thus larger depletion and electric field. In the TJ2, the 3T readout structure has been modified to allow for faster readout, of the order of a few ns, and the large pitch pixels have a reduced spacing between the electronics and the collection electrode to improve charge collection.

Our project Ph.D. student, Håkan Wennlöf, has commissioned the new readout system for the TJ1b and TJ2. A new carrier board is available that allows eTCT measurements. This carrier board required a change to most of the hardware in the setup. The current setup, shown in Fig. 1, does not feature custom developed FPGA and analogue cards as for the TJ1 setup. High voltage for the sensor and power for the electronics are supplied directly by external PSUs. The bias currents for the readout transistors are provided via resistors on the carrier boards. The default values of the resistors needed to be changed to provide the correct bias current and operate the chips with the correct noise level. The reset signal is provided by an Arduino microcontroller. The output of the pixel is fed into a CIVIDEC amplifier and readout

via a DRS4 oscilloscope, as in the previous setup. We are now at the stage where we can correctly bias and run the TJ1b chip. We just received a TJ2 chip and we expect to have results from this by the meeting in January.

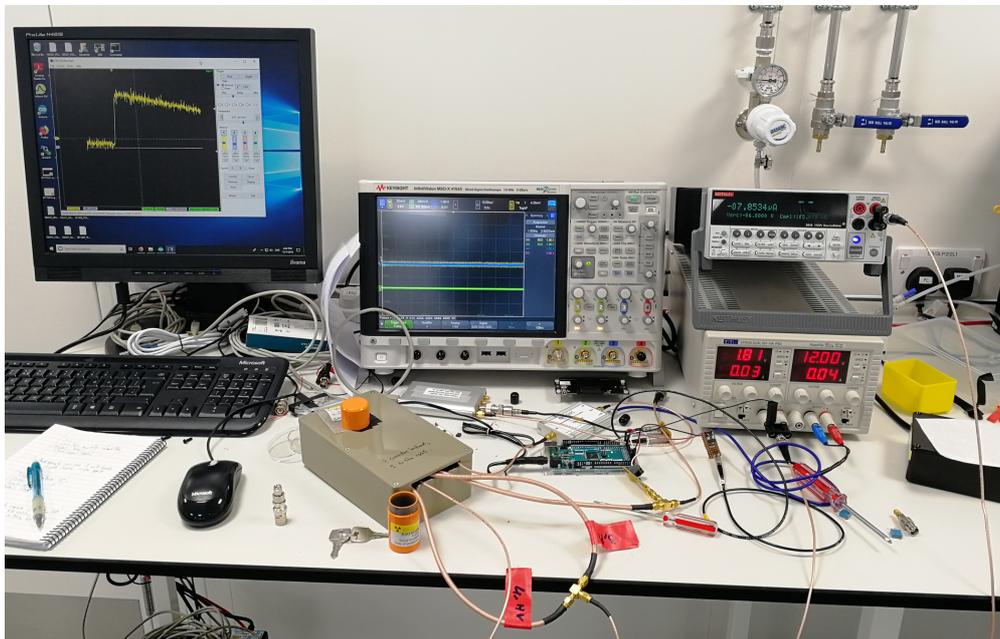


Figure 1: Setup for tests of the TJ1b and TJ2 chips with radioactive sources.

First preliminary results have been obtained with TJ1b for the  $28 \times 28 \mu\text{m}^2$  pixel matrix. Results agree with those obtained with the TJ1 for the same bias voltage of -6V on the p-substrate and p-well, as expected. Figure 2 shows a histogram of the signal amplitude for different voltages applied to the p-substrate measured with an  $^{55}\text{Fe}$  source. The p-well is kept at -6 V as in previous measurements with the TJ1. The data have been acquired with the same number of triggers for each bias setting.

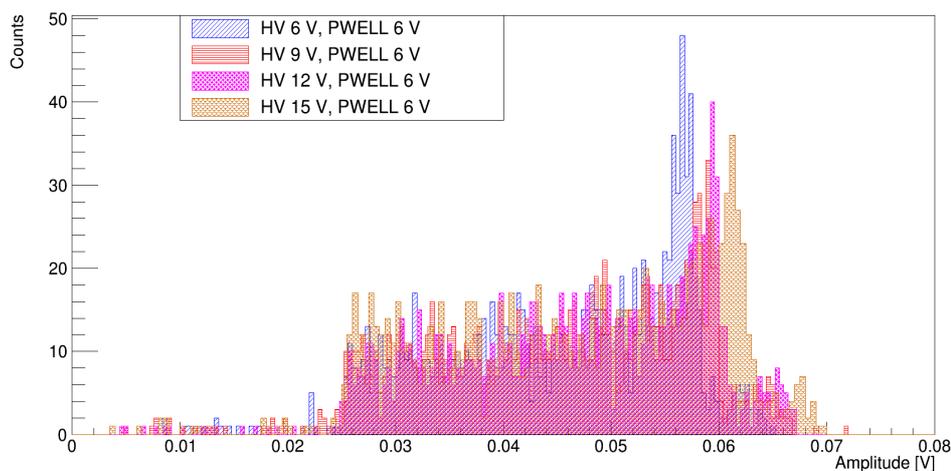


Figure 2: histogram of signal amplitude for the  $28 \times 28 \mu\text{m}^2$  pixel matrix of the TJ1b measured with an  $^{55}\text{Fe}$  source.

The plot shows that the gain depends upon the applied HV: the amplitude of the  $K_{\alpha}$  peak increases with larger voltages applied to the p-substrate. The histogram also shows an increased sensitivity to small hits. This is possibly due to the larger electric field at the edges of the pixel that allows the collection of charges generated in this area and thus shared among pixels. This explanation is supported by the measurement of the rise time of the signal. A larger collection time is measured for higher voltages indicating the collection of charge with larger drift paths.

Table 1: mean collection time and distribution width for the  $28 \times 28 \mu\text{m}^2$  pixel matrix of the TJ1b measured with an  $^{55}\text{Fe}$  source.

<b>HV bias [V]</b>	<b>Mean collection time [ns]</b>	<b>Distribution width [ns]</b>
-6	$24.34 \pm 0.09$	$2.817 \pm 0.072$
-9	$25.95 \pm 0.09$	$2.969 \pm 0.082$
-12	$27.52 \pm 0.12$	$3.943 \pm 0.098$
-15	$29.42 \pm 0.17$	$4.889 \pm 0.123$

Measurements are ongoing to understand whether there is a lower sensitivity to large hits or if the decrease of the  $K_{\alpha}$  peak is due to the fact that the measurements were carried out for the same number of trigger signals for each bias condition.

It is worth noting that these studies are part of a larger characterisation programme carried out by CERN, Birmingham and Oxford to understand the modified process, and that for this specific foundry run, results obtained with the MALTA sensor (one of the DMAPS prototypes for the ATLAS pixel ITk upgrade, submitted together with the TJ1b and TJ2) after irradiation are not in agreement with what was measured with the TJ1. Further investigations are needed, not only with radioactive sources but also eTCT measurements, to understand all observed features. Future tests are discussed in section 2.1.

The second aspect of WP1 are the EIC sensor design studies. We have been meeting with chip designers at RAL to define a workplan and deliverables. As presented in our previous report, two complementary designs are considered: a tracking and vertexing sensor achieving the highest possible spatial resolution, and a tracking and timing sensor providing a time-stamping capability with potentially lower spatial resolution. In the interest of setting a demanding specification, we will first attempt to design a sensor that meets the requirements of both cases simultaneously, based on a  $20 \mu\text{m}$  pitch pixel, timing resolution down to 1 ns, and with strict power budget constraints. In discussion with the designers at RAL, the target for the latter has been set to  $< 10 \text{ mW}/\text{cm}^2$ . Table 2 shows an updated list of specifications. As the project progresses, we will evaluate whether descoping options are needed: relaxing power specifications (although not higher than the  $20 \text{ mW}/\text{cm}^2$  power consumption of the ALPIDE for the innermost layers of the ALICE ITS), or designing two different sensors, one optimised for vertexing and tracking, and the other optimised for timing.

Table 2: Updated specifications for an EIC DMAPS sensor. An interaction rate of 500kHz is assumed to obtain the integration time. The timing resolution for the timing detector assumes bunch crossing frequencies of 112.6 MHz for eRHIC and 748.5 MHz JLEIC, and that each bunch crossing needs to be tagged as this would be the worst case.

	<b>EIC DMAPS Sensor</b>	
<b>Detector</b>	Vertex and Tracking	Outer Timing Layer
<b>Technology</b>	TJ or similar	
<b>Substrate Resistivity [kOhm cm]</b>	1	
<b>Collection Electrode</b>	small	
<b>Detector Capacitance [fF]</b>	<5	
<b>Chip size[cm x cm]</b>	Full reticule	
<b>Pixel size[um x um]</b>	20 x 20	<b>TBD</b>
<b>Integration Time [ns]</b>	2000	2000
<b>Particle Rate [kHz/mm<sup>2</sup>]</b>	<b>TBD</b>	
<b>Readout Architecture</b>	Asynchronous	<b>TBD</b>
<b>Power [mW/cm<sup>2</sup>]</b>	<10	
<b>NIEL [1MeV n<sub>eq</sub>/cm<sup>2</sup>]</b>	10 <sup>^</sup> 10	
<b>TID [Mrad]</b>	<10	
<b>Noise [e-]</b>	<b>TBD</b>	
<b>Fake Hit Rate [hits/s]</b>	<b>TBD</b>	
<b>Interface Requirements</b>	<b>TBD</b>	
<b>Timing Resolution [ns]</b>	N/A	<9 (eRHIC) <1 (JLEIC)

The work is split into four stages: literature review, pixel design, readout design, global effects studies. A report will be generated at the end of the study and shared with the EIC R&D Detector Advisory Committee. Figure A.1 in the appendix shows a Gantt chart with the planned phases of work with RAL. All documents have been prepared at RAL, and contracts and financial agreements are being put in place in anticipation of a start in January 2019.

#### WP2 – Layout simulations

Most of the work carried out in the last 5 months has been on the sensor development work package (WP1). However, some progress has also been made on the layout simulations. We have performed two studies: one varying the pixel pitch in the proposed outer timing layer of the silicon barrel, and the second incorporating the forward disks into the layout simulations.

At the July meeting we presented a study of the impact of adding a relatively thick (1.6% X/X<sub>0</sub>) outer timing layer on the momentum resolution and impact parameter resolution of pions in the transverse momentum range 0-5 GeV/c. The pixel size in that study was the same 20 x 20 μm<sup>2</sup> for all silicon layers. We have now defined the outer timing layer as an independent detector volume within EicRoot so that its pixel size (spatial resolution) can be varied independently of the other layers. This study

has shown that both momentum resolution and impact parameter (pointing) resolution is largely insensitive to the spatial resolution of the timing layer. This was expected since the momentum resolution is mainly a function of total track length and the impact parameter resolution depends strongly on the spatial resolution and radial position of the innermost layer. These results are not discussed further here.

With regard to integration studies with eRD16, we have begun to investigate the impact of positioning the first disk within the silicon barrel. A schematic diagram showing the initial arrangement of the barrel and the disks is shown in Fig. 3.

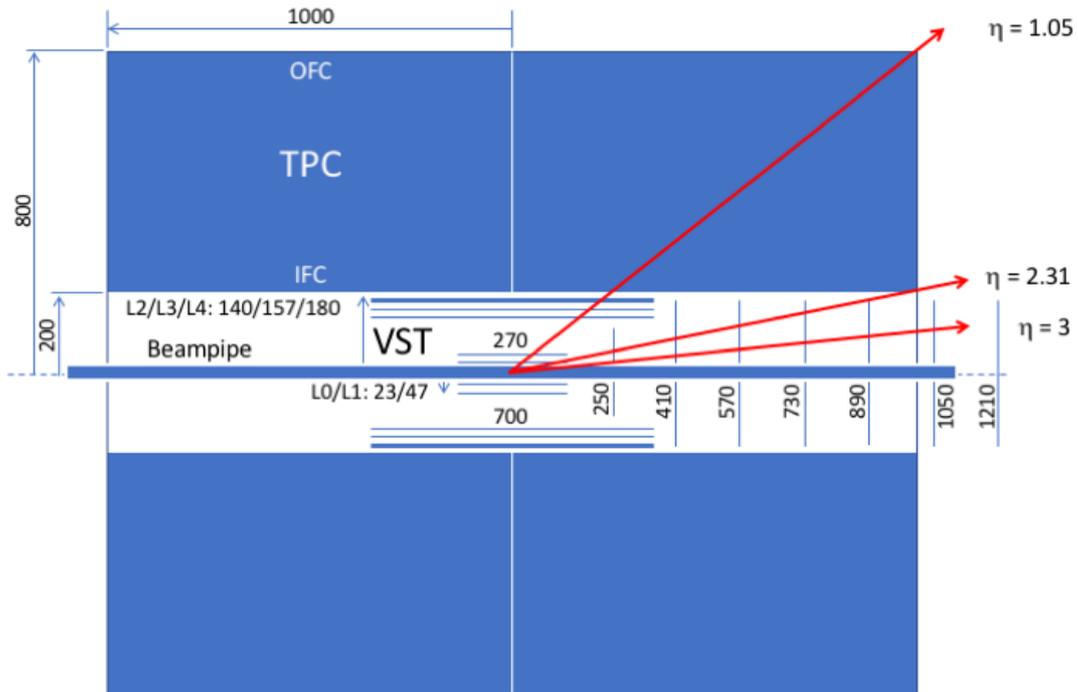


Figure 3. Simulation layout illustrating the position of the VST tracking layers labelled L0-L4 and the forward disks. The disks are shown on one side only. (All dimensions in mm.)

Seven disks are shown, equally spaced between 250 mm and 1210 mm from the nominal interaction point. Studies will be performed investigating the optimal position of the first disk. The current arrangement allows direct comparison with results obtained by eRD16 in the LDT simulation framework. To benchmark our simulation against the results obtained by eRD16 [1], we have simulated electrons at a fixed pseudorapidity of  $\eta = 3$ , in the momentum range 0-50 GeV/c and with a magnetic field strength of  $B = 3$  Tesla for a variety of pixel sizes. Figure 4 shows a comparison of the relative momentum resolution ( $\Delta p/p$ ) as a function of momentum.

The simulations are generally in agreement apart from the EicRoot simulation missing the obvious upturn at low momentum observed by eRD16 and which is believed to be due to the effect of scattering in the beampipe. The impact of the beampipe has been tested in EicRoot by scaling the thickness of the beampipe by a factor of ten, which

enhances the negative tail in the relative momentum distribution as expected. The origin of this discrepancy is currently under investigation.

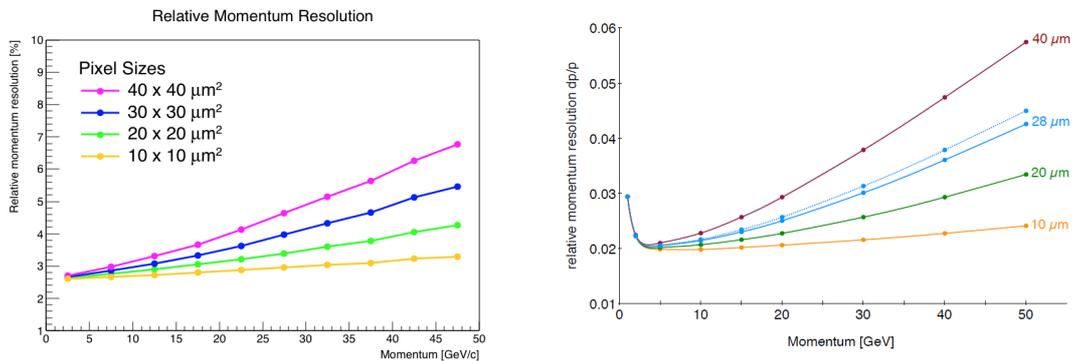


Figure 4. The relative momentum resolution of electrons at pseudorapidity  $\eta = 3$  for various pixel sizes. The left panel shows results from an EicRoot simulation (this work). The right panel shows results from eRD16 using the LDT framework. Both simulations incorporate a beryllium beampipe of thickness 0.8 mm.

### 1.3 What was not achieved, why not, and what will be done to correct?

We believe the project is on track at this stage.

## 2 Future

### 2.1 What is planned for the next funding cycle and beyond? How, if at all, is this planning different from the original plan?

For the remainder of FY19 we will be working on completing the proposed programme of work in both work packages.

For WP1, we aim at having a full characterisation of the modified TJ 180 nm CMOS process. This will consist of results from different pixel matrices, from all three TJ investigator chips, obtained both with radioactive sources and with eTCT measurements to study not only the charge collection properties, but also the depth and profile of the depletion region. At the same time, we will work with the chip designers at RAL according to the plan outlined above. We aim to have the report on studies of pixel design and readout architectures, and an updated list of specifications by the July meeting.

For WP2, we aim to study momentum resolution and impact parameter resolution as a function of pseudorapidity and by varying the position of the first and second disks. This may include asymmetric designs, created by shortening the inner silicon barrel layers in the direction of the scattered electron. We will continue to work with eRD16 to work out the best disk and barrel configuration.

## 2.2 What are critical issues?

No critical issues to report at this stage.

## 3 Manpower

*Include a list of the existing manpower and what approximate fraction each has spent on the project. If students and/or postdocs were funded through the R&D, please state where they were located and who supervised their work.*

Prof. Peter Jones (0.05 FTE) – no cost to project

Dr. Laura Gonella (0.1 FTE) – no cost to project

Håkan Wennlöf (1.0 FTE) – PhD student, funded by the University of Birmingham

Prof. Phil Allport and Prof. Paul Newman have had an advisory role and participate in our regular project meetings to monitor progress.

## 4 External Funding

*Describe what external funding was obtained, if any. The report must clarify what has been accomplished with the EIC R&D funds and what came as a contribution from potential collaborators.*

EIC R&D (FY17) funds supported a postdoc for 5.5 months, which enabled us to make a start on the detector layout simulations within the EicRoot software framework.

EIC R&D (FY18) funds supported the travel of the project members to the EIC generic detector R&D meetings and EIC UG meeting. It also paid for Håkan Wennlöf to travel to CERN to work with collaborators on the TJ technology, and to participate in the “Third Barcelona Techno Week – Course on Semiconductor Detectors”. The remaining funds of FY18 will be used together with FY19 funds to pay for the sensor design work at RAL.

This project receives the support of a PhD student funded by the University of Birmingham. In addition, we have recently learned that our bid to support some of the R&D elements of this proposal through EU Horizon 2020 has been successful. This formed part of the NextDIS work package included in the STRONG-2020 proposal. We are still waiting to hear details about the financial settlement.

## 5 Publications

*Please provide a list of publications coming out of the R&D effort.*

Not applicable at this stage of the project.

## 6 References

[1] E. Sichtermann *et al.*, eRD16 presentation, EIC Detector R&D Meeting, July 2018.

Appendix

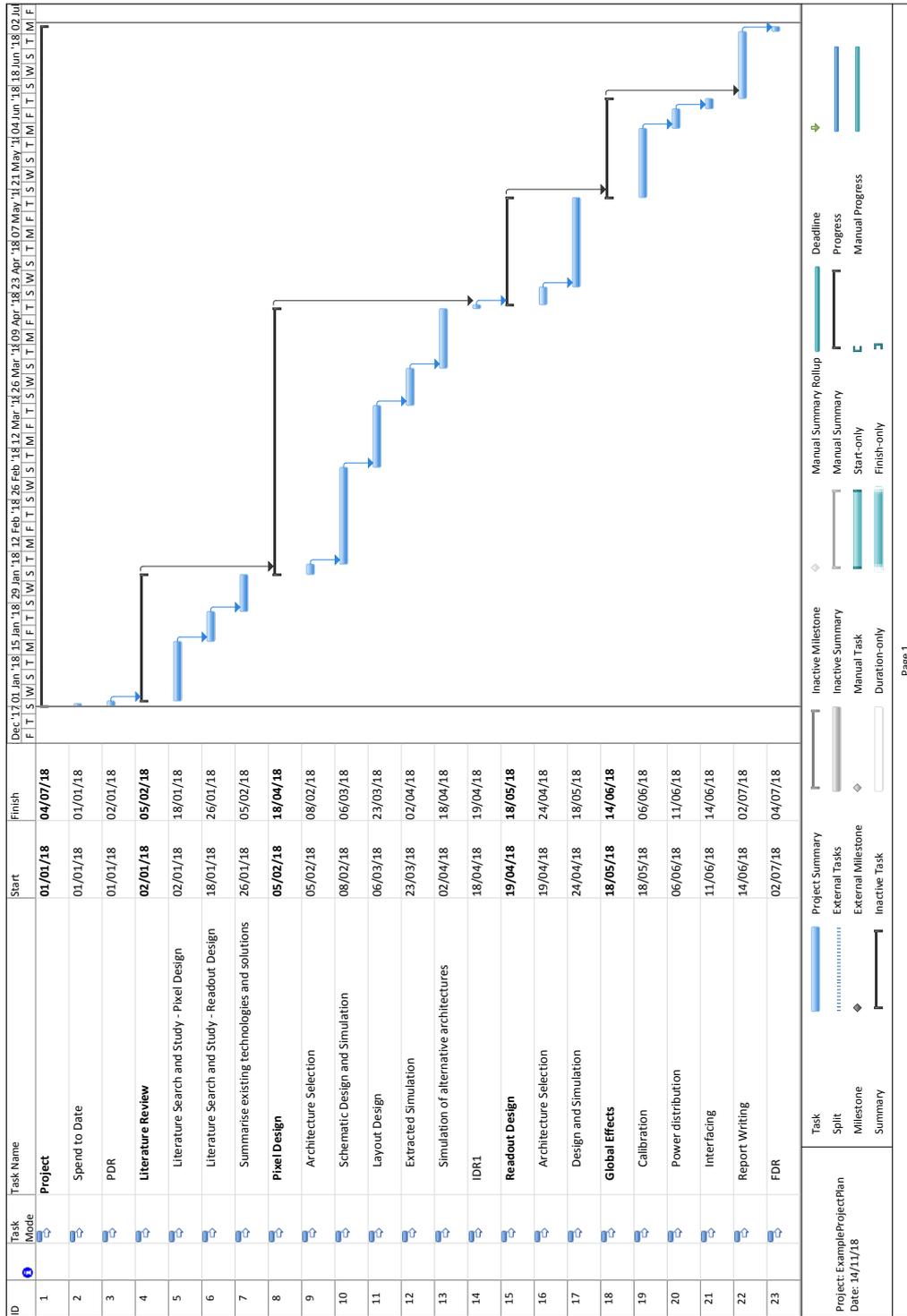


Figure A.1: Workplan for the feasibility study of an EIC DMAPS sensor