# Research and Development of a Silicon-based Tracker System for the Detector of the Electron-Ion Collider

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Two preliminary detector designs [1] have been proposed for the electron-ion collider (EIC). To achieve the physics program, both designs call for tracking detectors, the type of which is based on the radial distance from the interaction point. Closest to the interaction point, silicon-based tracking systems are to be implemented. This proposal is for the research of operational features for a silicon-based tracking system and its compatibility with a curved Micromegas tracking detector.

Silicon detectors are ideally suited for tracking close to the interaction region as they are capable of handling high rates and a high radiation dose. They provide exceptionally good vertex and tracking resolutions, and they are reliable. These characteristics are evidenced by their ubiquitiousness in high-energy physics laboratories across the world.

Jefferson Lab and collaborators, Moscow State University, Russia, and the University of New Hampshire, have been involved in the design, development, and implementation of a silicon vertex tracker (SVT) for the upgrade of the CLAS detector in Hall B at Jefferson Lab [2, 3].

The upgrade of CLAS is motivated by research interest in: spectroscopic studies of excited baryons' influence of nuclear matter on propagating quarks, polarized and unpolarized quark distributions, and comprehensive measurements of generalized parton distributions.

Many of the experiments deal with electro-production of exclusive and semi-inclusive final states. Cross-sections for these processes are small, necessitating high-luminosity experiments to achieve the desired statistical accuracy in a few months of data-taking; a number of experiments rely on running at a luminosity of $10^{35}$ $cm^{-2}s^{-1}$.

The SVT, which has ~34,000 channels, provides polar angle θ coverage for tracking from 35° to 125°. The azimuthal angle φ coverage is ~2π. To unambiguously identify a missing pion in exclusive processes in the central tracking system, which consists of the central time-of-flight detector and the SVT, the fractional momentum resolution at a momentum of 1 GeV is required to be 50 MeV. To determine individual vector components of the momentum at the 25 MeV level, the central tracker's angular resolution in φ is required to be of the order of 5 mrad. These variables are summarized in Table I.

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| Variable | Value |
|---|---|
| Angular coverage | 35°–125° |
| Momentum resolution | $dp/p < 5\%$ |
| θ resolution | 5–10 mrad |
| φ resolution | 5 mrad/sin θ |
| Luminosity | $10^{35}$ $cm^{-2}s^{-1}$ |

TABLE I. SVT variable values.

As shown in Fig. 1, the SVT will be centered inside the 1800-mm long solenoid that has an outer and inner diameter of 2040 mm and 780 mm, respectively, and a maximum central field of 5 T. In the forward region, the tracker is constrained by the high threshold Cerenkov counter (HTCC).

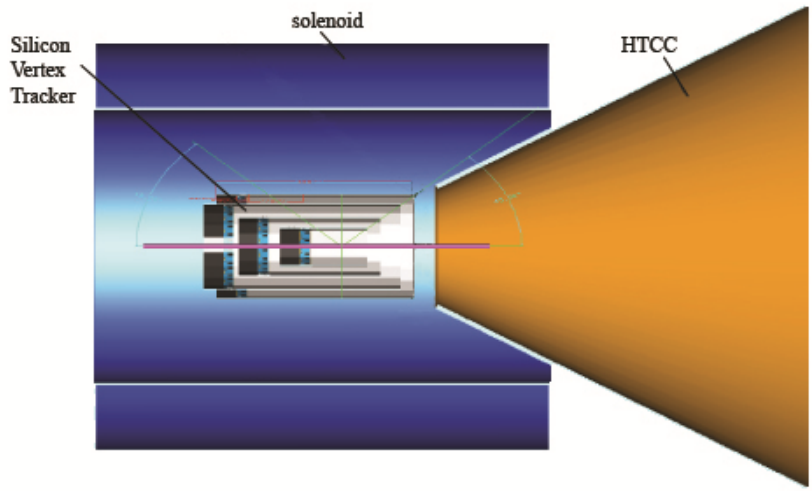


FIG. 1. Location of the SVT in the solenoid.

Conceptual design studies on the silicon tracker started in 2004 [4]. Several configurations of the SVT were studied [5–12] with the aim to optimize the layout with respect to operability, performance, and cost. The final design, Fig. 2, has four regions, each with 10, 14, 18, and 24 sectors, respectively.

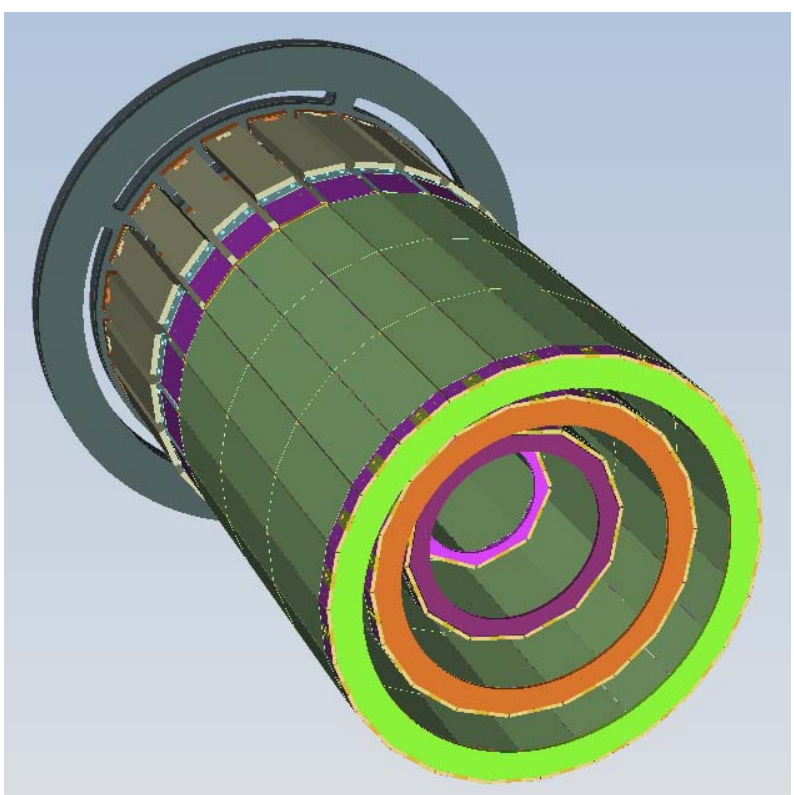

FIG. 2. The end view of the SVT detector.

The present plan is to replace the fourth region by a six-layer, curved Micromegas detector. Simulations indicate that this configuration, three silicon double layers and three Micromegas double layers, dramatically improves the vertex, angular, and tracking resolutions. In this case, the three regions of the SVT will be limited in the radial extent to 140 mm, beyond which the Micromegas detector is located. The clearance between the SVT and the Micromegas detector is ~16 mm.

Event and background rates were estimated using GEANT4 [13–15]. These studies indicate that on region one of the silicon tracker, the maximum rate, including electromagnetic background, for a full-field (5 T) setting of the solenoid, is ~60 MHz.

The sectors (modules) that make up each of the regions of the silicon tracker are identical, Fig. 3. Single-sided silicon sensors, manufactured by Hamamatsu of Japan, each of which is ~11cm long and 4.2 cm wide, with a readout pitch, at the H sensor end, of 156 µm, sandwich the backing structure made of Rohacell, carbon fiber, bus cable, and heat sink. Each module has three types of sensors, Hybrid, Intermediate, and Far. The readout strips have graded angles—read-out strip #1 is parallel to the longitudinal axis of the module and the last readout strip, strip #256, has an angle of $3^{o}$ with respect to the longitudinal axis of the module. The angle between two consecutive readout strips increases by $1/85^{th}$ of a degree. Front-end readout is facilitated by a flex circuit board instrumented with the Fermilab Silicon Strip Readout – Version 2 (FSSR2) ASICs [16].

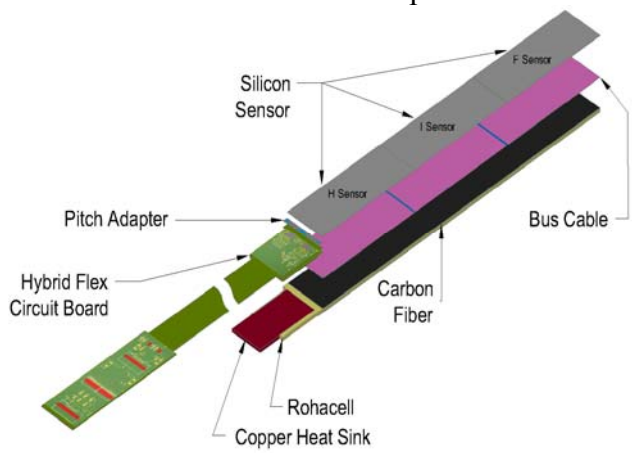


FIG. 3. SVT module.

FSSR2 has a data-driven architecture. Hence, it requires no external triggering to read out the data. The ASIC was fabricated by the Taiwan Semiconductor Manufacturing Company in the 0.25-µm CMOS process. The block diagram of the FSSR2 ASIC is shown in Fig.4.

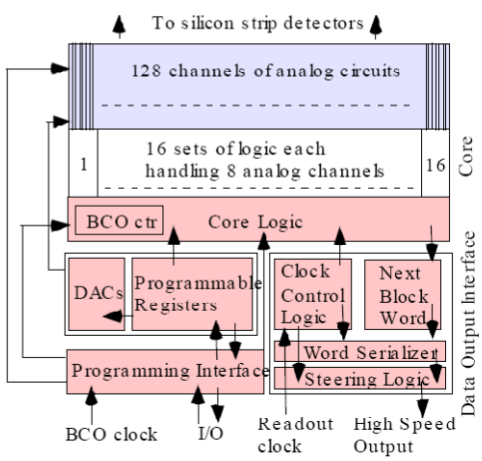


Fig.4 FSSR2 block diagram.

Internally, the ASIC has four main sections: FSSR2 core, data output interface, programming interface, and programmable registers.

The core has 128 analog channels which are subdivided into 16 columns, each with eight analog readout strip inputs. For the data acquisition clock setting of 132 ns, the readout architecture can handle with efficiency greater than 99%, a 2% strip signal occupancy. If a hit is detected in one of the channels, the core logic transmits pulse amplitude, channel number, and time stamp information to the data output interface.
The data output interface accepts data transmitted by the core, serializes it, and transmits it to the data acquisition system. The number of serial data lines for the output is programmable. To send the 24-bit readout words, one, two, four, or six data lines can be used. Both edges of the 70-MHz readout clock are used to clock data to provide the maximum output data rate of 840 Mb/s over the six low voltage differential signal lines. The readout clock is independent of the acquisition clock [17].

The programming interface handles the slow controls communication link between the ASIC and the data acquisition system. The internal programmable registers, accessed via the programming interface, are used to set up the ASIC and provide control functions.

At the present time, we have built several modules, in cooperation with Fermilab, and instrumented these modules with state-of-the-art hybrid flex circuit boards and tested them at our facility. In the course of building and testing these modules, we have gained extensive experience in the subject matter.

For the EIC silicon tracking system, we propose to build, initially, a 66-cm long module—two standard modules placed end to end—and read out from both ends. Additionally, we plan to investigate the mechanical stability of the long module and determine how to maximize the signal-to-noise ratio of the module.

The Micromegas detector for the CLAS12 upgrade is being built by CEA Saclay - Irfu, France. CEA is already part of the EIC-approved research and development project [18]. Since, the detector for the EIC is to be equipped with a silicon-based tracking system, which is to work in conjunction with a Micromegas detector, we are of the opinion that the study of the compatibility of a silicon-based vertex tracking system with the Micromegas tracking system is crucial. To this end, we plan to conduct extensive tests, including a full-'scale test with the CLAS SVT and the CLAS Micromegas, to understand and optimize the compatibility of these two tracking detectors. This study should be beneficial towards understanding and building a complex tracking detector, one that comprises both silicon and Micromegas tracking detectors, for the detector of the EIC.

At Jefferson Lab, we have the needed facilities and infrastructure to perform the aforementioned tasks. We have a clas 10,000 cleanroom dedicated for module fabrication, and associated infrastructure, such as a granite table and a wire bonder, as well as test and measurement equipment, such as a probe station and a dark box needed to evaluate the silicon modules and Micromegas prototypes, and necessary peripherals, such as the environmental chamber and the dry-storage systems.

For these endeavors, for manpower, labor, and materials, we request a funding of $247,000. Table II, below gives a breakdown of our funding request.

| | Year 1 | Year 2 | Year 3 | Total |
|---|---|---|---|---|
| Post-doc | K$50 | K$50 | K$50 | K$150 |
| Hardware | K$25 | K$25 | K$25 | K$75 |
| Travel | K$8 | K$7 | K$7 | K$22 |
| Total | K$83 | K$82 | K$82 | K$247 |

Table II: Breakdown of funding request.

Our three-year plan is as follows:

Year 1: Recruit post-doc, procure backing structure materials for the silicon module, build module, test module performance, and work on optimizing signal-to-noise ratio.

Year 2: Procure necessary components to install the silicon module in close proximity to a curved Micromegas prototype and start compatibility tests.

Year 3: Complete compatibility tests on the module and the Micromegas prototype, and proceed to full-scale compatibility studies with the CLAS SVT and the CLAS Micromegas.

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