Planar Si sensors with optimized dead area and improved radiation hardness

The EIC Tracking and Calorimetry R&D

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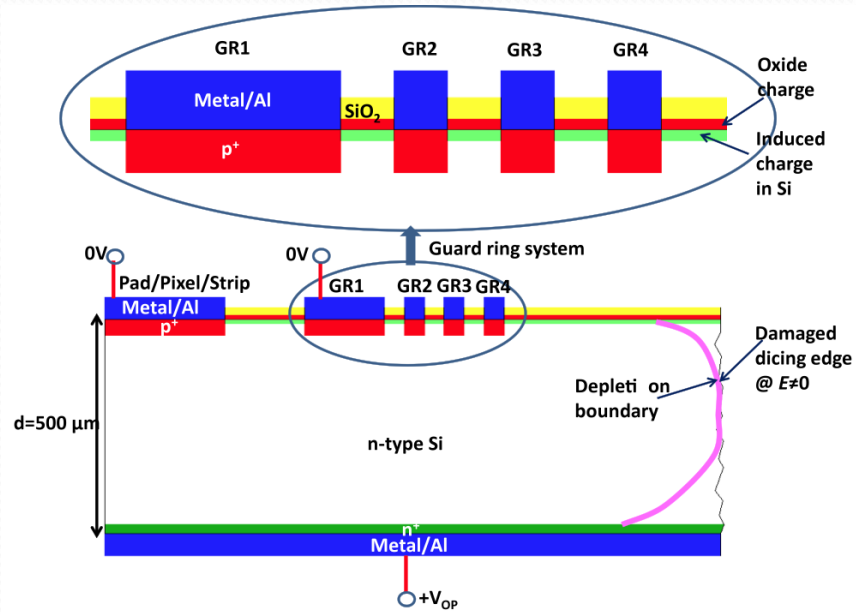
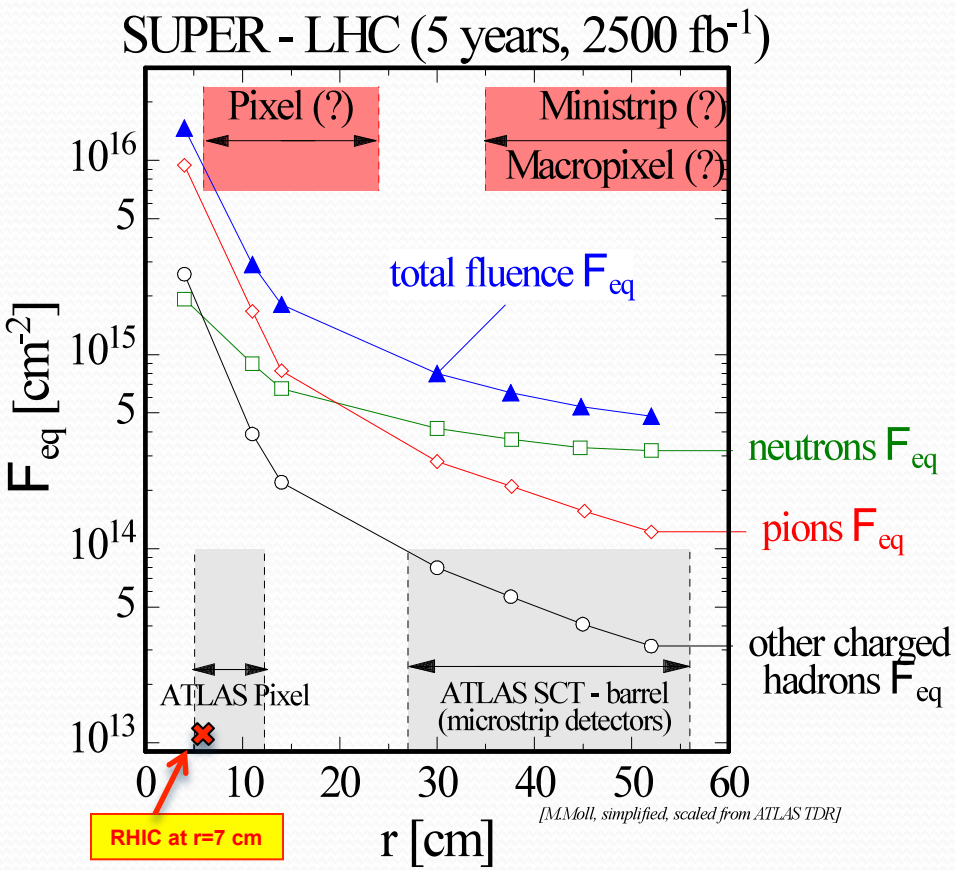
Off-shelf Si-sensors

Hamamatsu (Japan);
Micron semiconductors (UK);
ELMA (Russia)
ON-Semi (Czech rep.)
ETRI (Korea)



- **Multiple guard rings to avoid potential punch-through and Si break-down;**
- **Extra guard area to keep depletion from reaching sensor edge (> d);**
- **Edge damage from diamond saw dicing few 100µm deep;**
- **Total dead area width ≥1.5mm;**
- **~10% of sensor area is left dead just to control leakage and avoid break-down;**

Si sensors are relatively radiation hard but every improvement to radiation hardness will count



- **Bulk (Crystal) damage (nonionizing)**
  - **displacement damage, built up of crystal defects**
- **Change of effective doping concentration (higher depletion voltage, under-depletion)**
- **Increase of leakage current (increase of shot noise, thermal runaway)**
- **Increase of charge carrier trapping (loss of charge)**

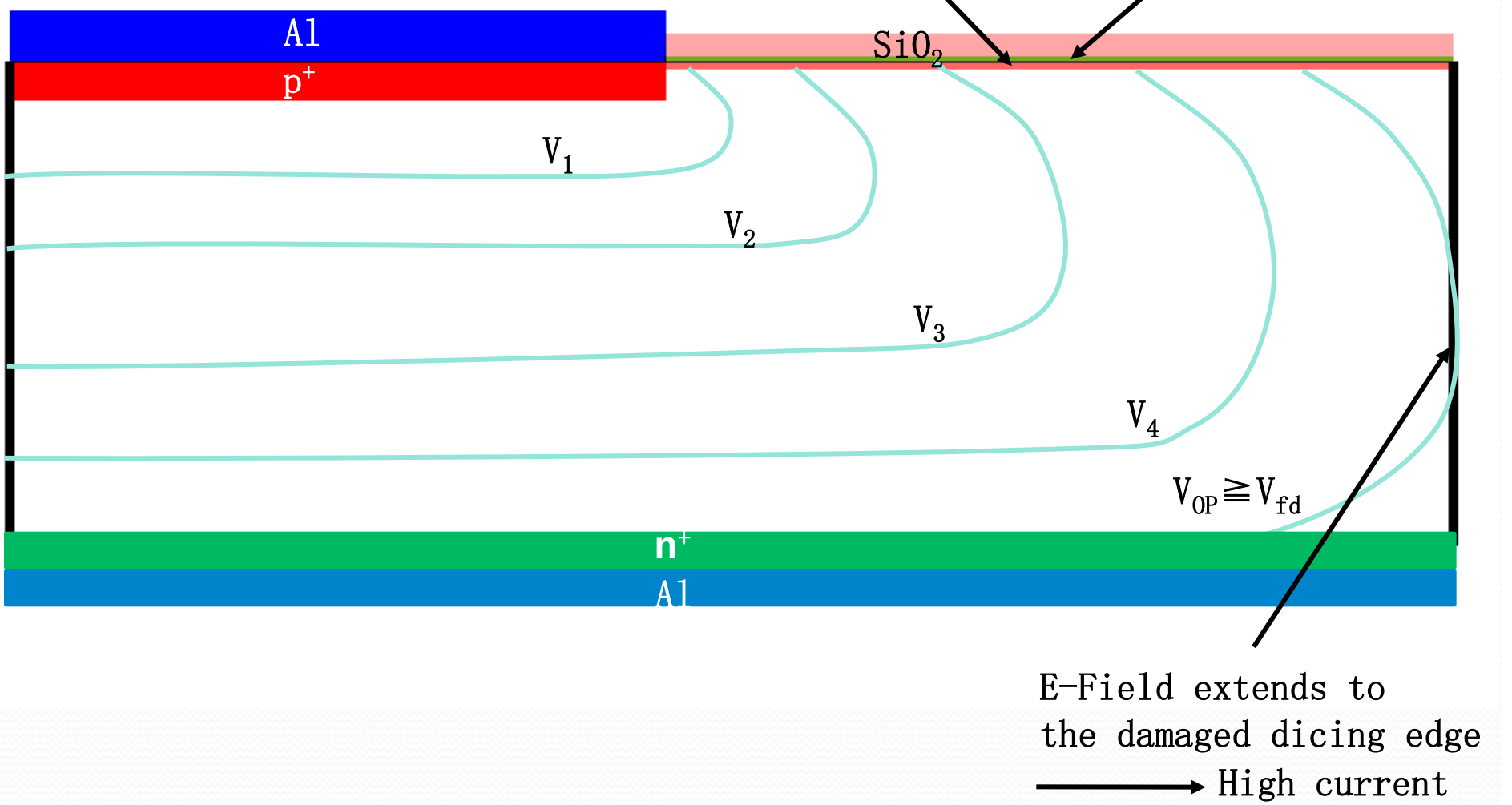
- **Surface damage due to Ionizing Energy Loss**
  accumulation of positive charge in the oxide (SiO_2) and the Si/SiO_2 interface

affects: interdiod capacitance (noise factor), breakdown behavior, …

Potential profile for bad oxide Charge

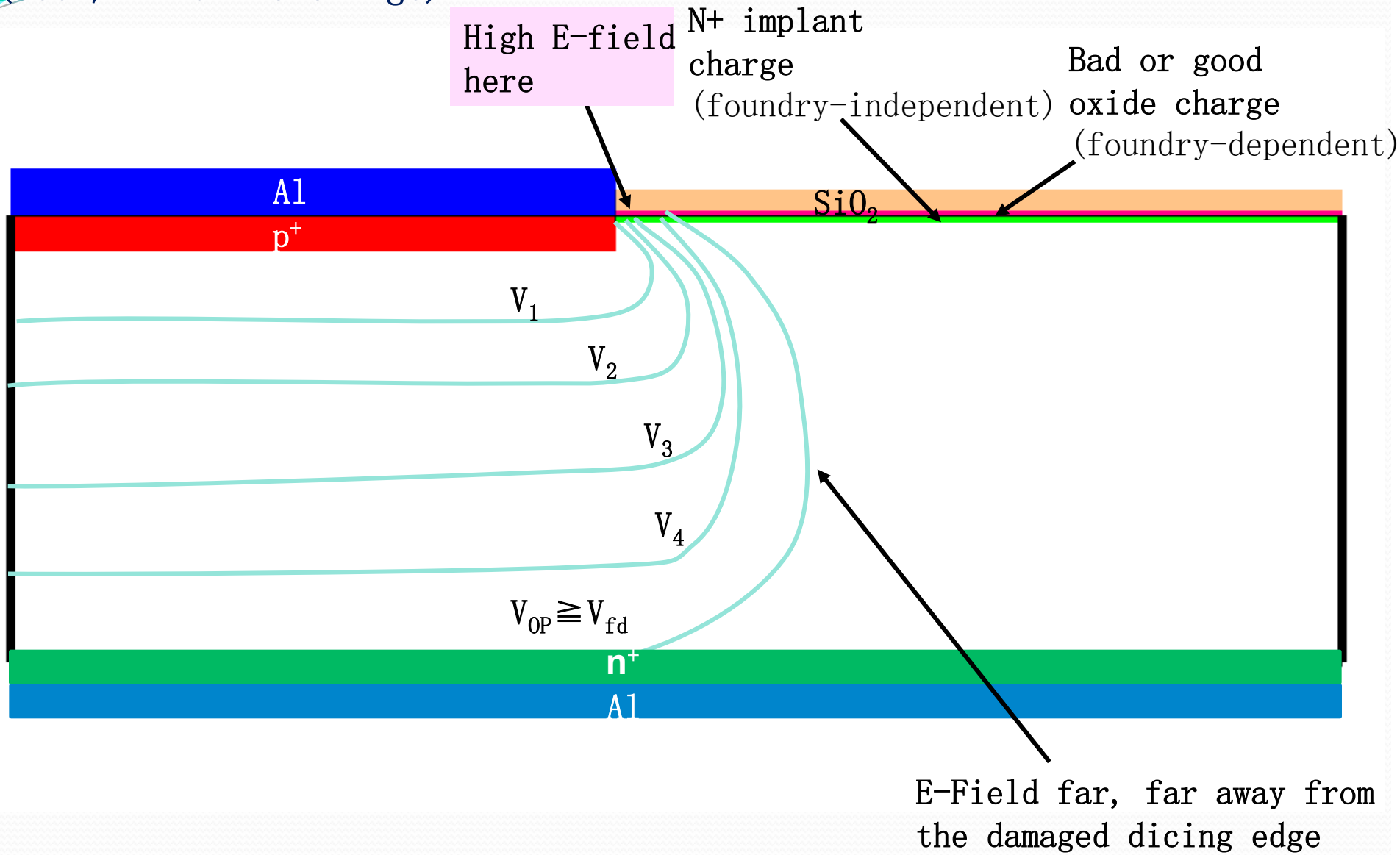
Oxide charge:

Goal	$2x10^{11}$ /cm
CMOS	~10^{10} /cm
Bad	can be negative

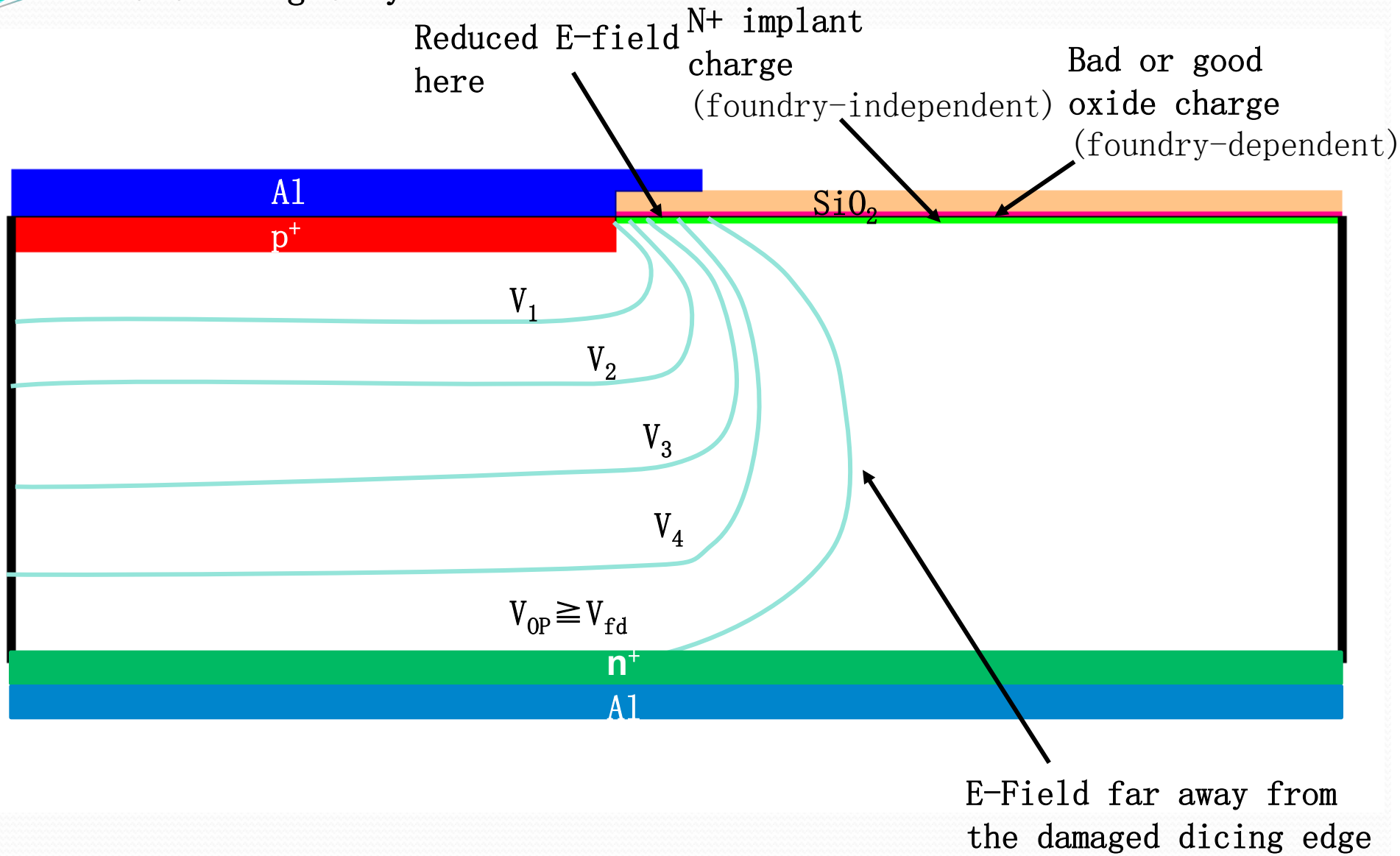


Potential profile with
N^+ implant layer (~dose=$1x10^{12}/cm^2$)
(Good/bad oxide charge)

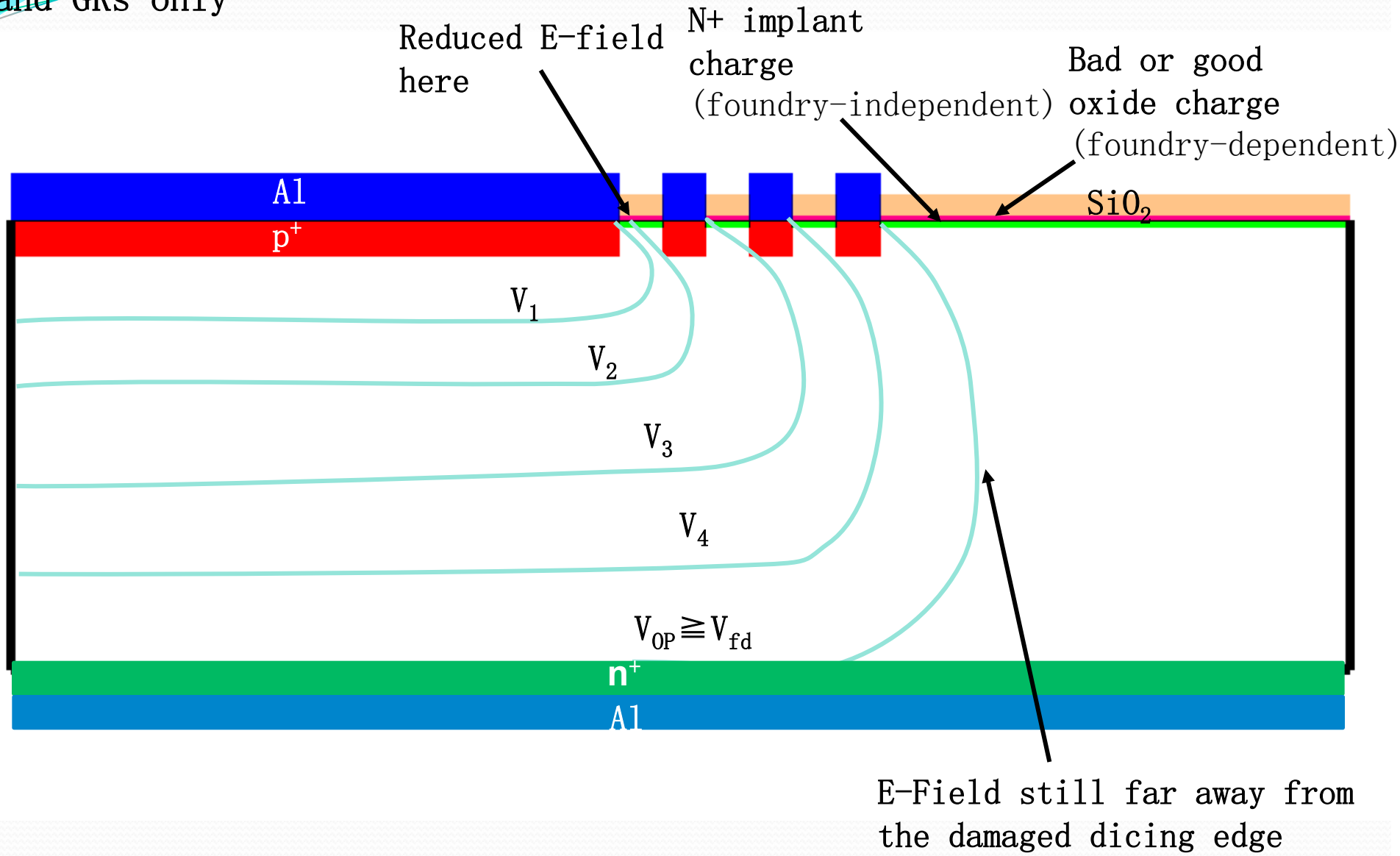
Control: N+ implant layer



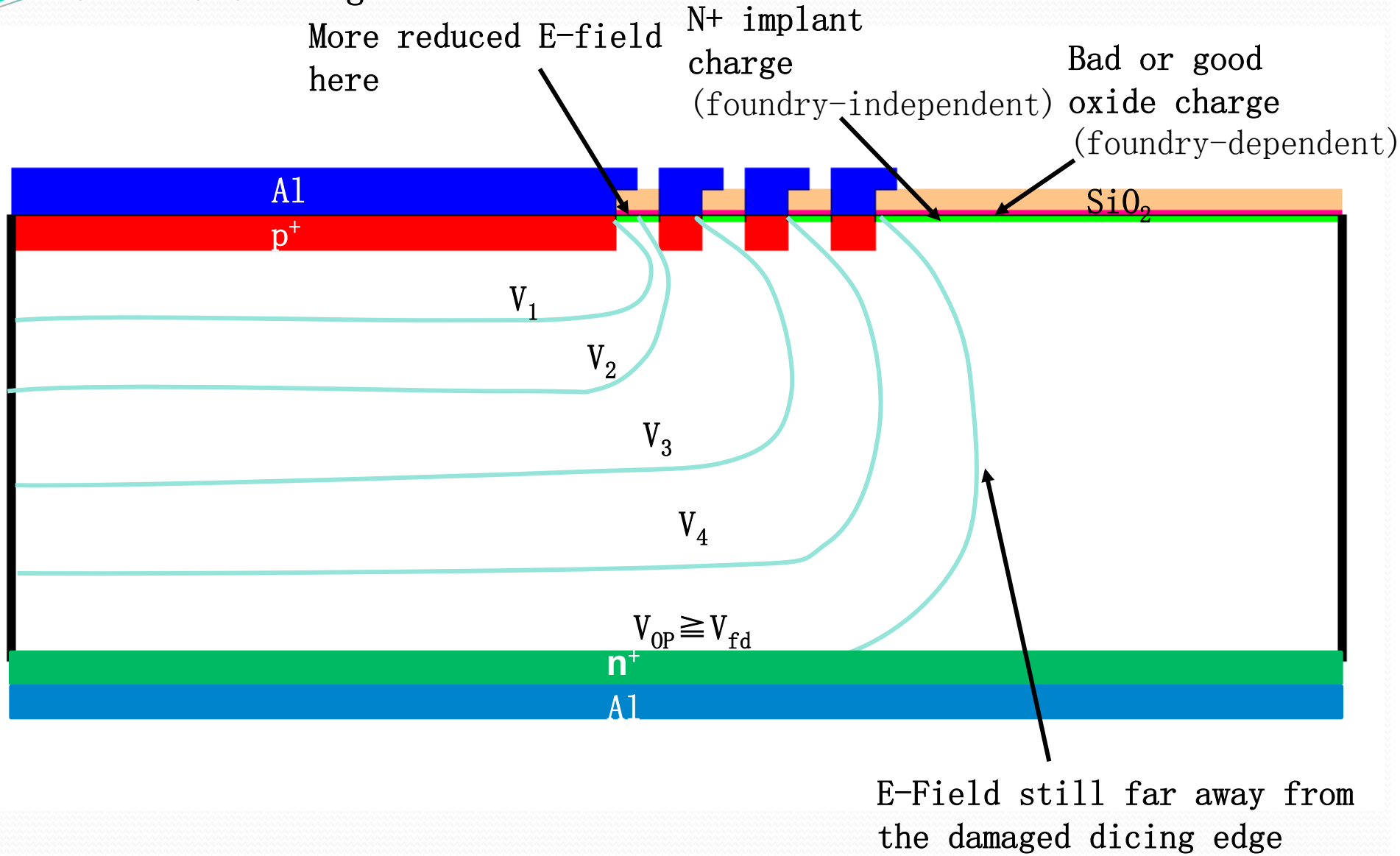
Potential profile with N^+ implant layer and Al over-hang only



Potential profile with N^+ implant layer and GRs only

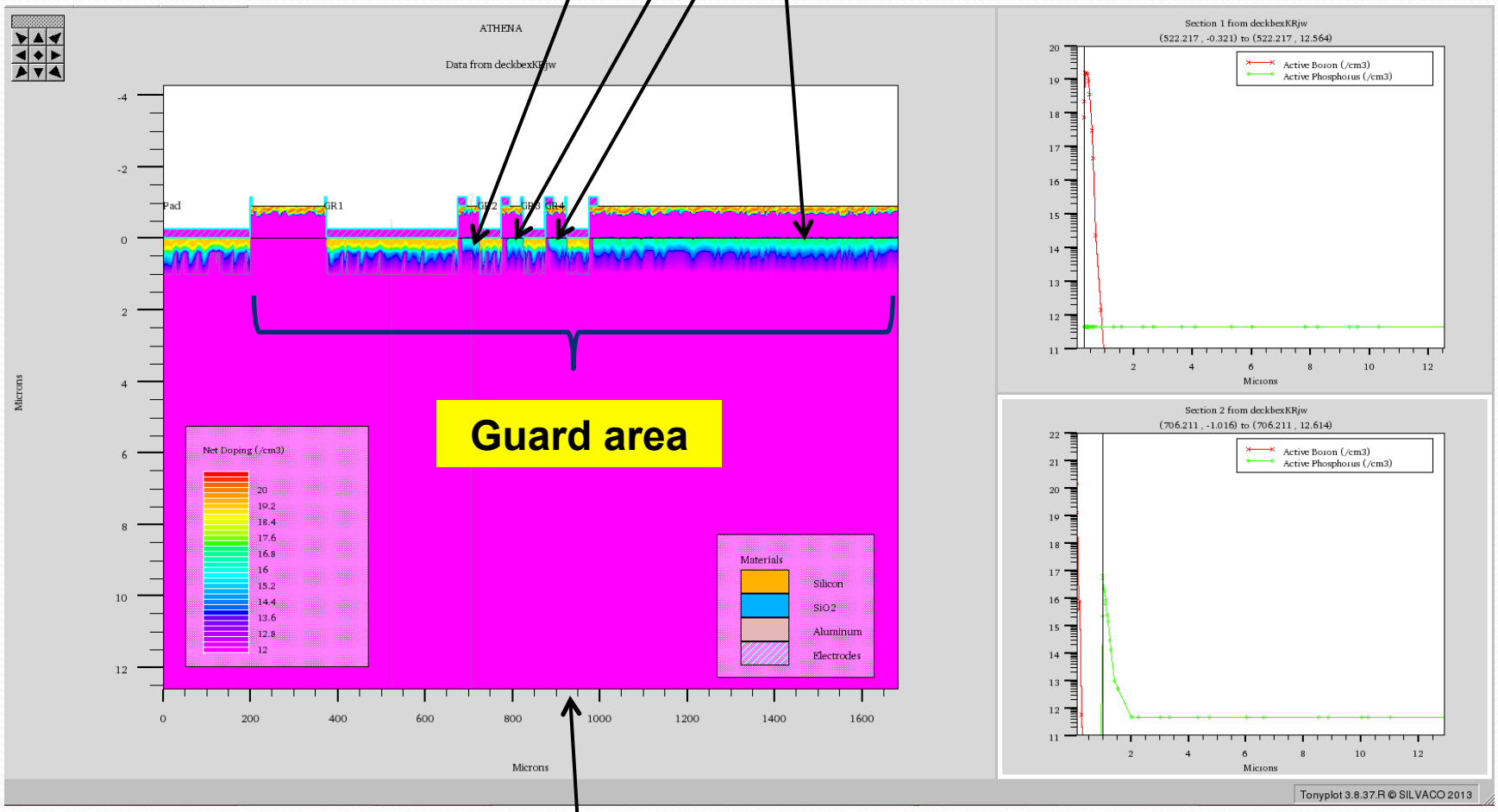


Potential profile with N^+ implant layer and GR+Al over-hang



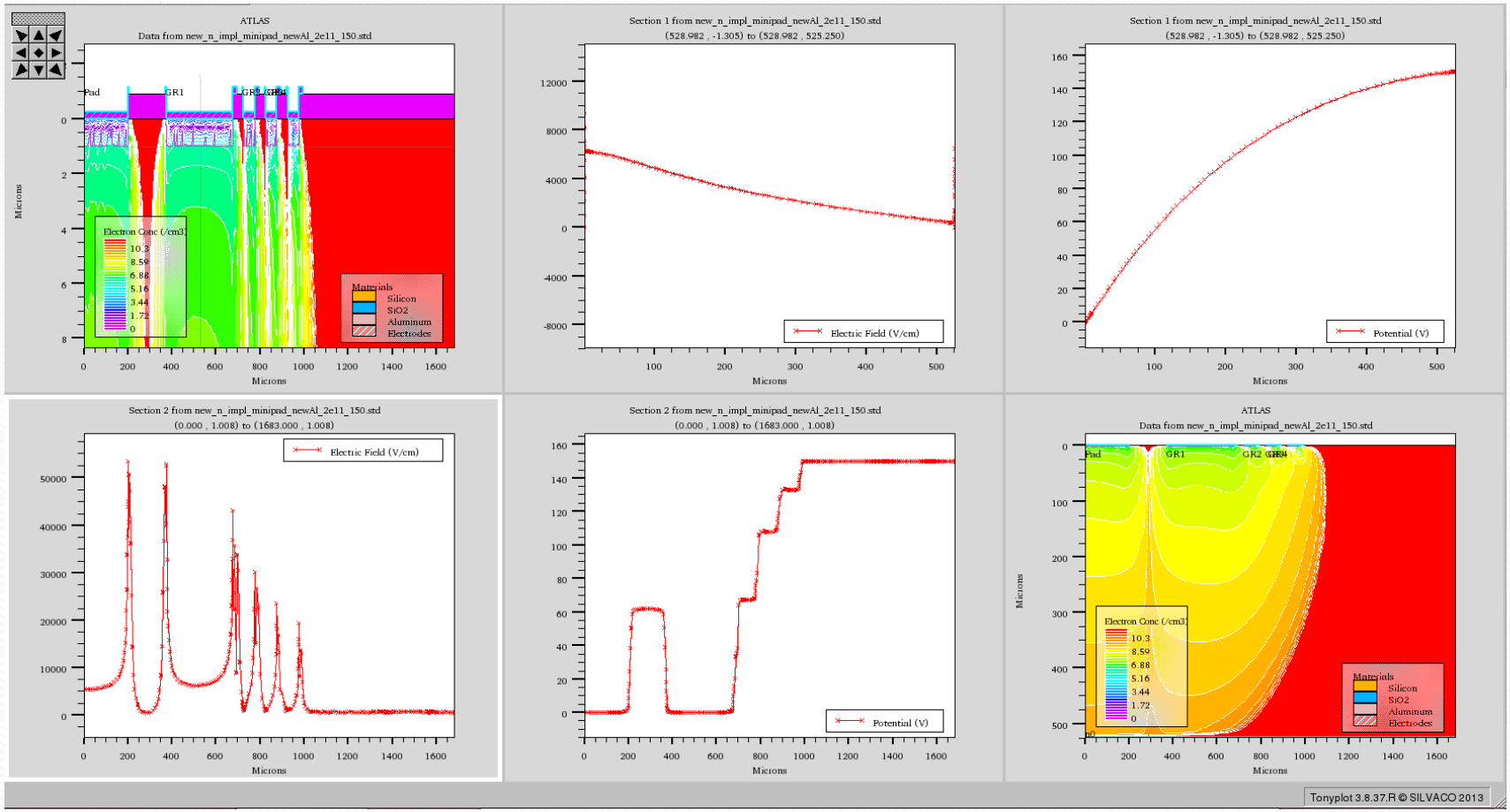
n^+ Implant (40 keV Ph, $1x10^{12}/cm^2$)

added in GR region ONLY

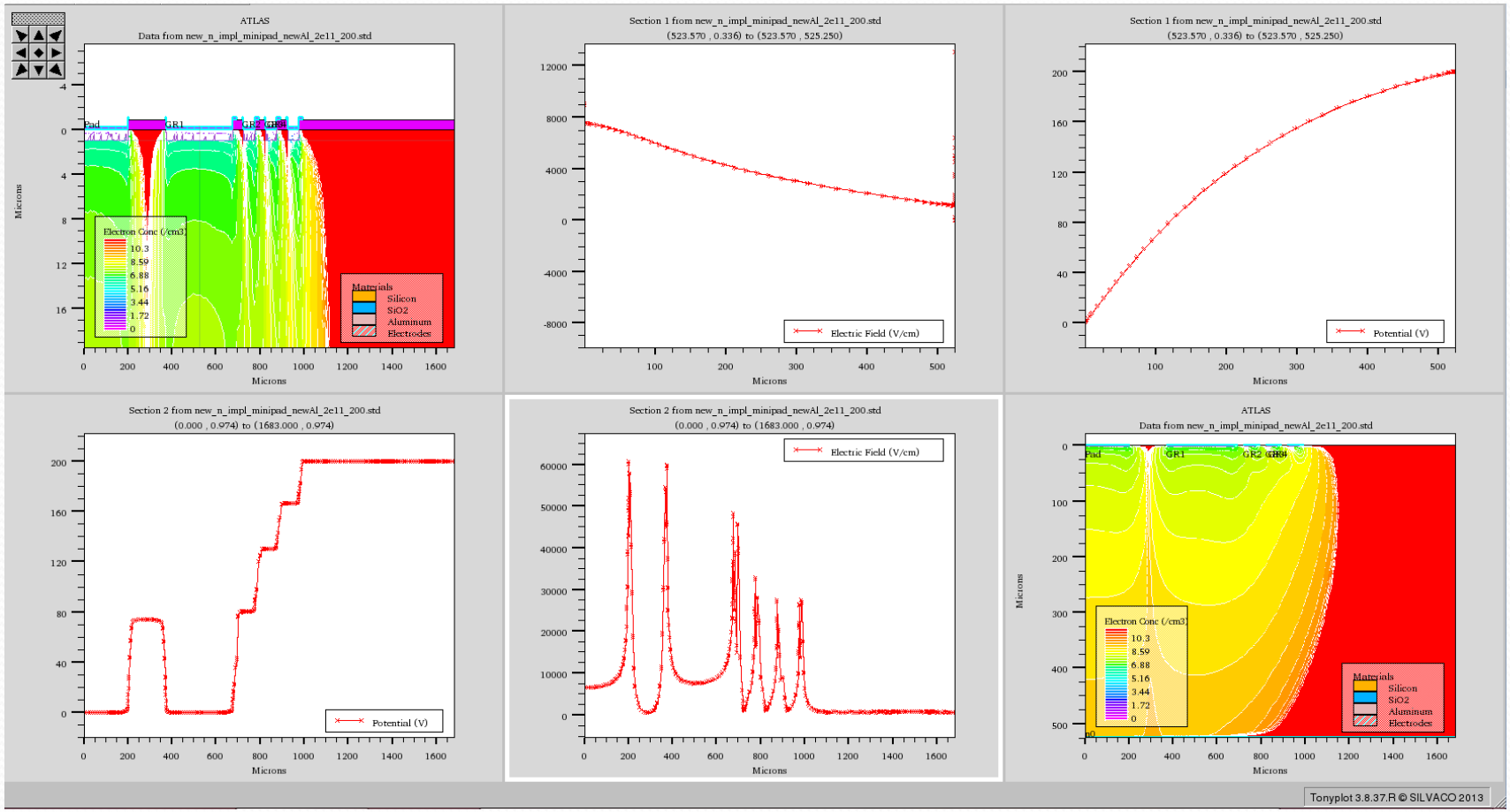


n^+ Implant (40 keV Ph, $1x10^{15}/cm^2$)

d=500μm; Vdep ~100V; N_{ox}=2x10^{11}/cm^2; Bias: 150 V

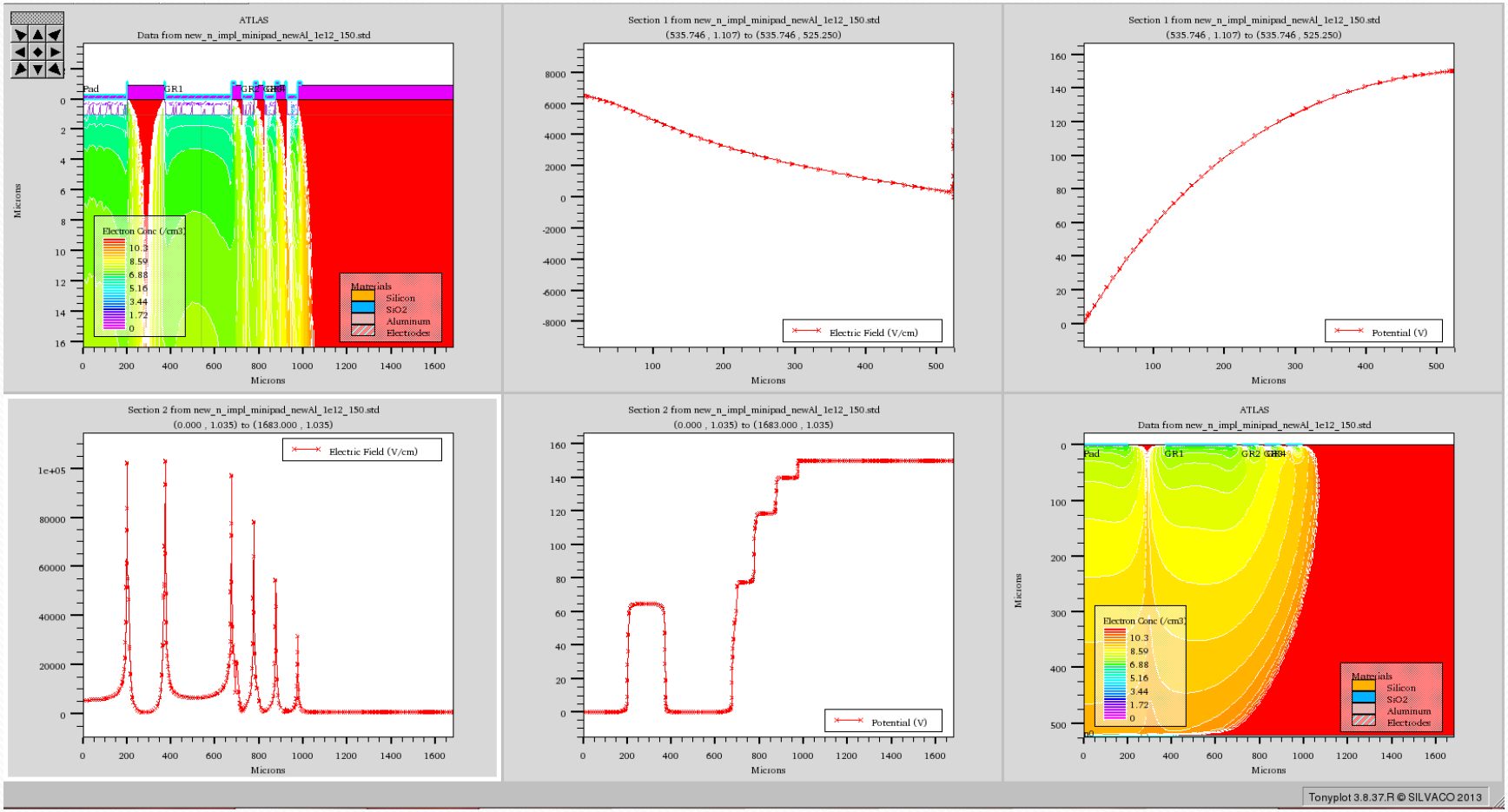


d=500μm; Vdep ~100V; N_{ox}=2x10^{11}/cm^2; Bias: 200 V (10 Mrad exposure equivalent)

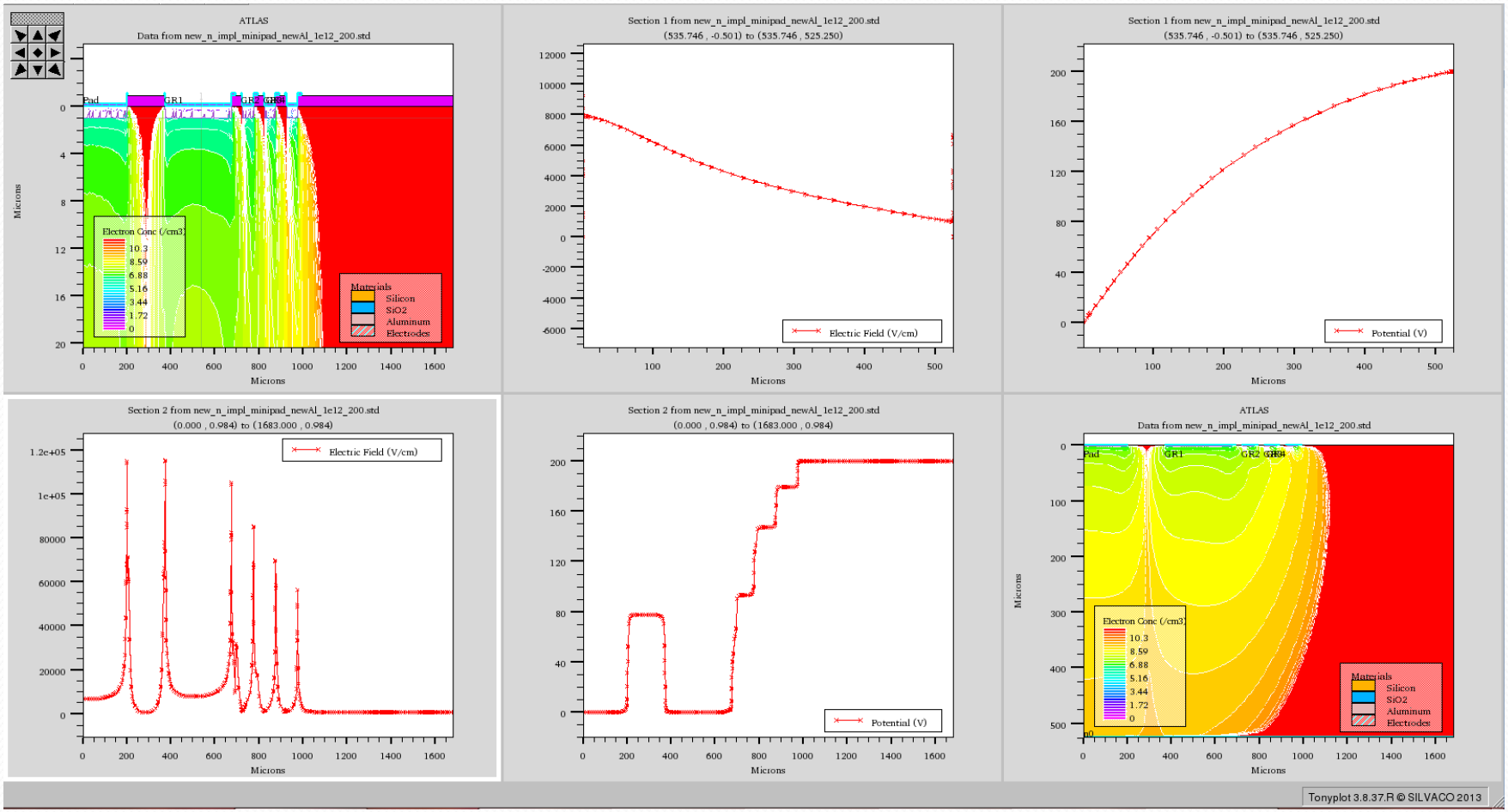


N_{ox}=2x10^{11}/cm^2 is the typical value for specialized foundries (including BNL)

d=500μm; Vdep ~100V; $N_{ox}=1x10^{12}/cm^2$; Bias: 150 V



d=500μm; Vdep ~100V; N_{ox}=1x10^{12}/cm^2; Bias: 200 V (10 Mrad exposure equivalent);



In all cases (up to 10 Mrad rad and 2 times the full depletion voltage)

1. Detector's maximum E-field is < breakdown field

2. The detector's lateral E-field is far away from the dicing edge

3. All of these are independent of detector foundry oxide quality

Summary of nearly "risk-free" R&D subjects

(1) To introduce N+ implant in the guard ring area as a mean to control blocking charge density: to make the GR system free from the punch-through without affecting the detector main sensitive region (pad/pixel/strip region) and no negative effects in the detector main body;

(2) To introduce a metal over-hang (in the order of 10's of microns) between P+ implanted guard rings over N+ implanted gaps: to spread the electric potential to a wider distance so to reduce the value of maximum electric field in the p+/n + interface area. Simulations have shown a reduction of about a factor of two in this maximum electric field;

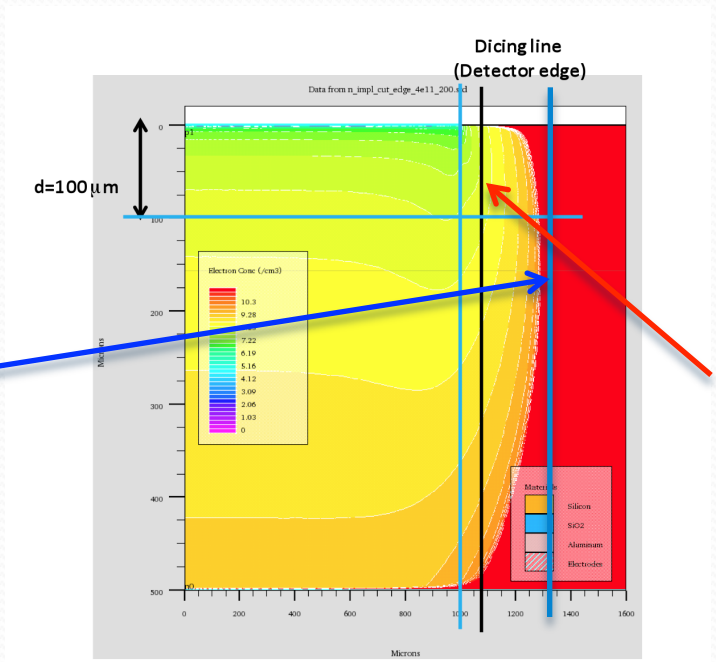
(3) To study further improvements to distribution of electric potential in the guard ring area: (example) replace a uniform N^+ implant in the GR area with segmented N^+ implant with a gap ($t_{gap} \geq 5\mu m$) of no N^+ implant near the outside edge of each GR;

High-risk R&D

To develop Si detectors with minimum dead edge area ("Thin Edge") by reducing the GR system with just one thin GR ("Thin GR"), or by eliminating the GR all together ("GR-Less"):

- **Laser dicing (damage limited to <10 μm wide);**
- **N+ implantation between sensitive area to dicing edge (hindering lateral depletion);**
- **Optimized geometry in interface regions.**

For 500 μm detector biased to 200 V (double of the full depletion voltage), the depletion edge is < 300 μm from the last pad/GR. With careful laser dicing, we can reduce the dead edge area to 300 μm.



Further examination gives us hints of how wide a thin dead edge we can obtain for thin detectors. At d=100 μm, the dead edge area can be as small as 75 μm.

Summary

- Proposed R&D program will result in
  - Improved quality and robustness of silicon sensors in general;
  - Increased efficiency of silicon coverage (reduction to dead areas);
  - Increased radiation tolerance of silicon sensors;
  - Design and implementation of the ultra-thin "Thin GR" and/or "GR-less" silicon sensors;
  - Reduction in cost – any good foundry will be eligible.
- Application areas:
  - Tracking (in particular forward tracking);
  - Calorimetry (preshower and energy sampler).

Budget

COST ELEMENT	FISCAL YEAR ___14__	FISCAL YEAR ____15_	FISCAL YEAR _16____	TOTAL COST
Salary: ½ PostDoc Salary: Technician	$ 25,000 $25,000	$ 26,000 $26,000	$27,000 $27,000	$78,000 $78,000
TECHNICAL SERVICES				
Materials Travel	$20,000 $5,100	$20,000 $5,900	$ - $7,000	$40,000 $18,000
Sub-contracts (Foundry Submissions)	$40,000	$40,000	$0	$80,000
TOTAL PROJECT COST Salary: Technical:				 $156,000 $138,000