UNIVERSITY OF BIRMINGHAM | SCHOOL OF PHYSICS AND ASTRONOMY

eRD18 - Precision Central Silicon Tracking & Vertexing for the EIC

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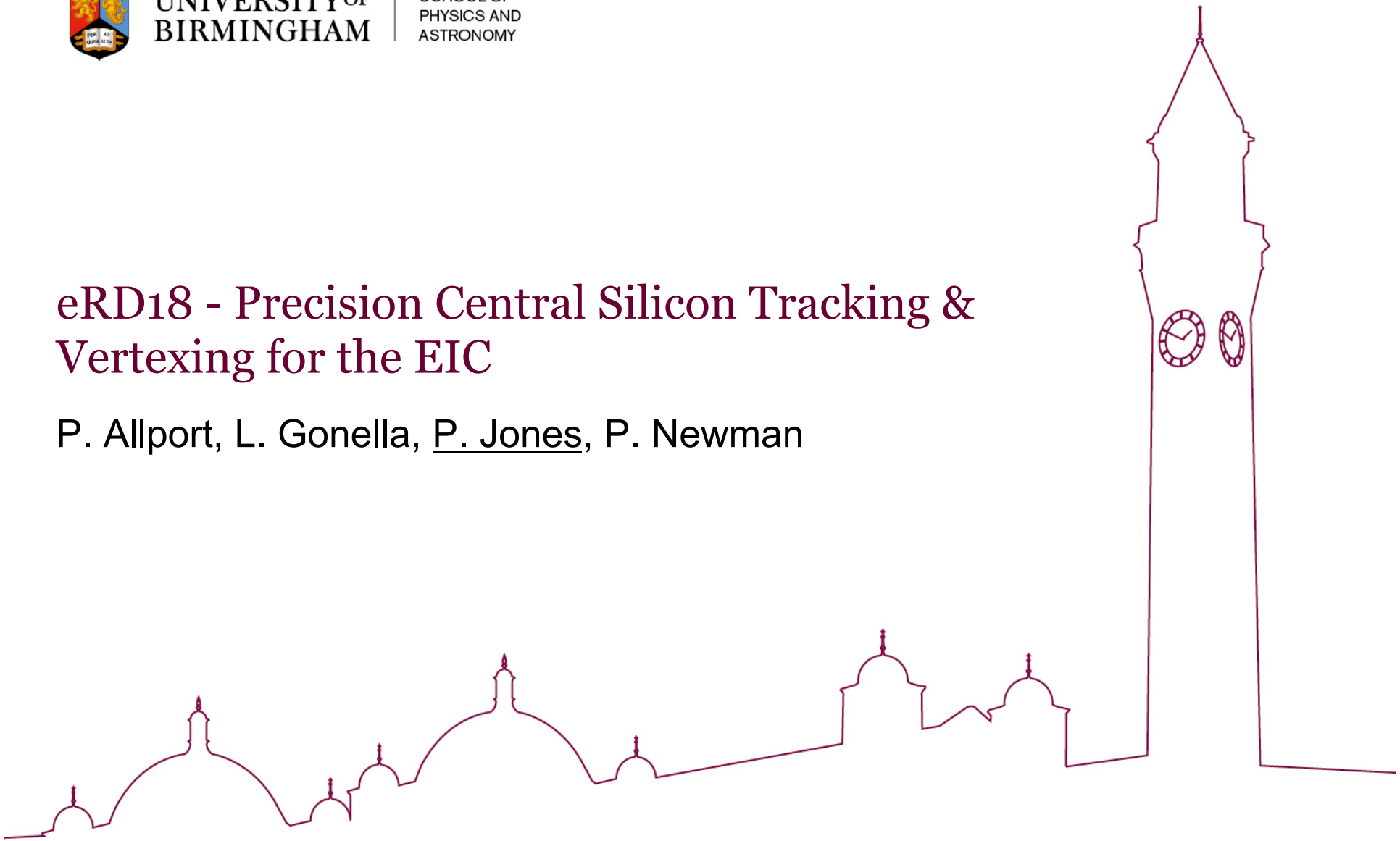


Original proposal

To develop a detailed concept for a central silicon vertex detector for a future EIC experiment, exploring the potential advantages of HV/HR-CMOS MAPS technologies

WP1: Sensor Development

Exploit on-going R&D in Birmingham into HV/HR-CMOS MAPS to investigate potential solutions for the EIC

WP2: Silicon Detector Layout Investigations

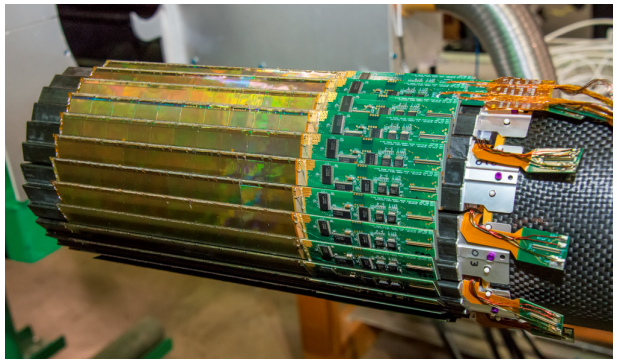
Performance characterisation with different assumptions on numbers of layers, layout and spatial resolution of the pixel hits

WP3: Physics Performance Evaluation

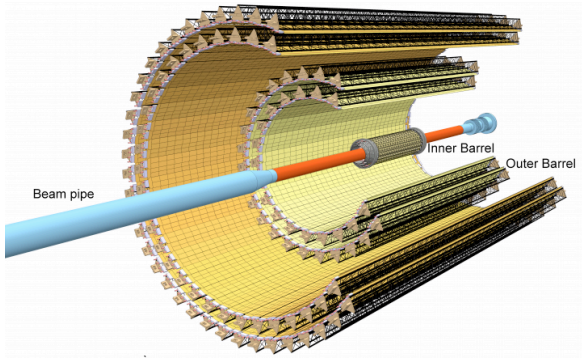
Propagation of performance into physics observables, particularly for heavy flavour physics

Background: State-of-the art MAPS

STAR Heavy Flavour Tracker (HFT) at RHIC

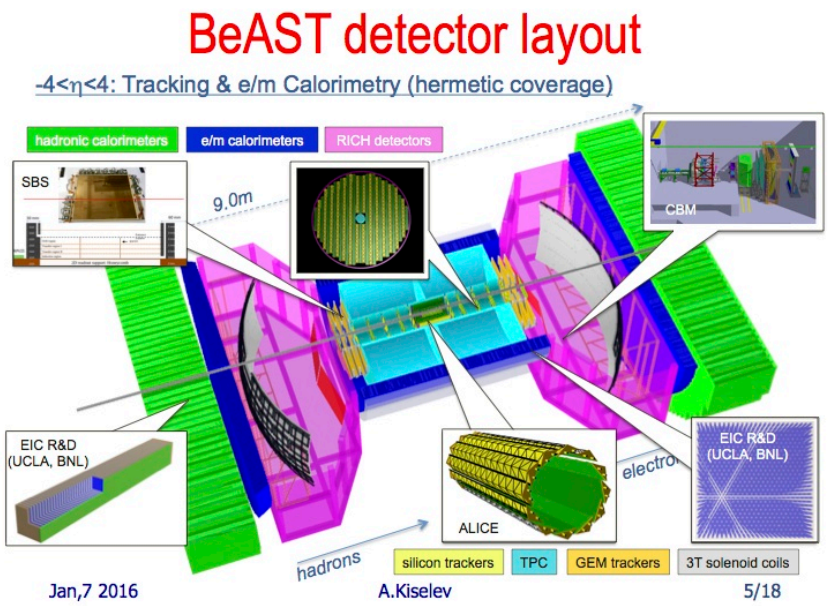


ALICE Inner Tracking System (ITS) Upgrade at LHC

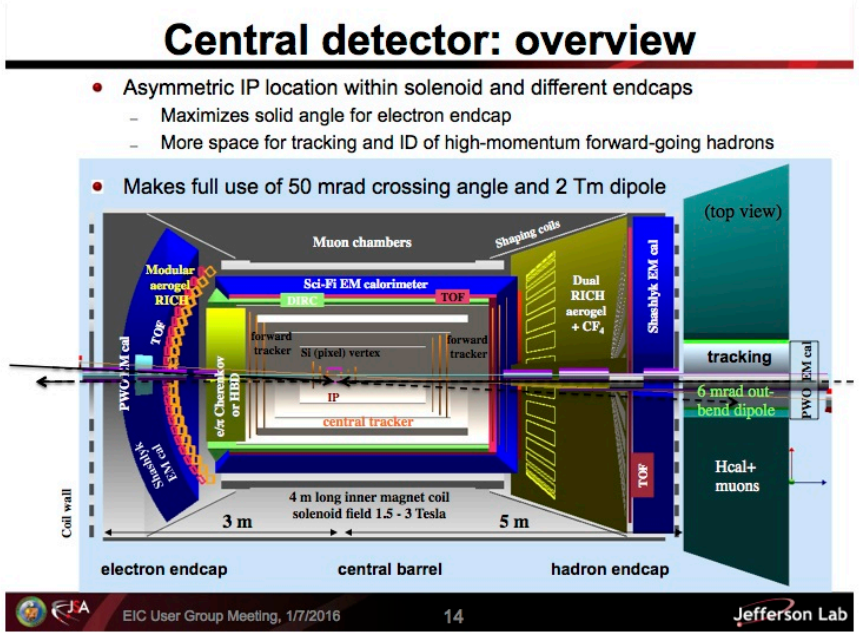


- Small pixel size (down to 20 μm x 20 μm)
- Low power (few hundred mW/cm^2)
- Low material budget (< 0.3% X_0)
- Moderate radiation hardness (~Mrad, 10^{13} 1MeV n_{eq}/cm^2)

Background: EIC Detector Concepts



Alexander Kiselev



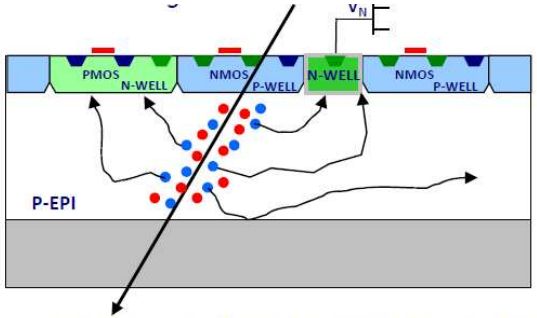
Pawel Nadel-Turonski

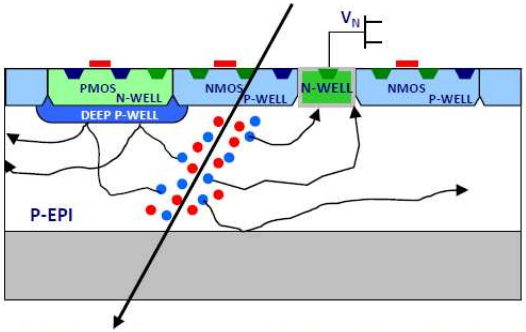
Based on **ALICE ITS** upgrade

Several technology options, e.g. **Belle II** DEPFET-based pixel **SVD**

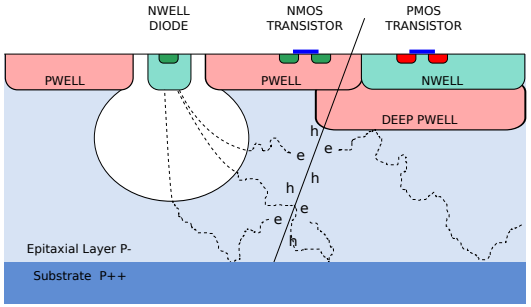
- Si vertex and tracker detectors in central and forward regions
- Seek high resolution, high s/n, low mass, low power solution

Background: Developments in MAPS





M. Winter, Terascale Workshop, Berlin, March 2015



J. Phys. G: Nucl. Part. Phys. 41 (2014) 087002

No depletion
NMOS only

→

No depletion
full CMOS

→

Depletion
full CMOS

Deep implants /
nested well

High Resistivity (**HR**) substrates
High Voltage (**HV**) transistors

plus smaller technology nodes and backside processing

↓

Depleted MAPS (or HV/HR-MAPS)

Background: Depleted MAPS

- Large number of R&D activities on depleted MAPS using HV/HR-CMOS technologies for particle tracking
  - Workshop on CMOS Active Pixel Sensors for Particle Tracking CPIX14, Bonn (Germany) 2014

- Charge collection by **drift**
  - Radiation hardness
  - Fast charge collection
  - Large collected charge
  - Small cluster multiplicity

→ Interesting for **high luminosity** proton colliders and fixed target

→ Interesting for **high precision** ion, lepton and lepton-hadron colliders

- **Full CMOS** in **small feature size** process
  - Larger choice of readout architecture
  - More integrated functionality

WP1: Sensor development

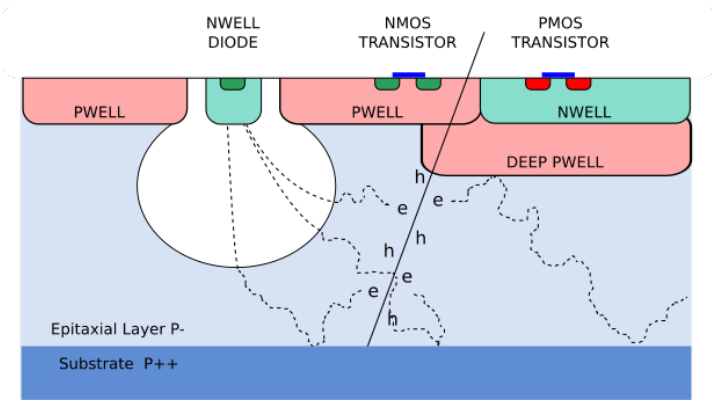
Aim

Demonstrate the possibility to achieve **higher spatial resolution** and **faster charge collection** in a **large depleted sensor volume**

R&D Strategy

Investigate two commercial **HV/HR-CMOS technologies**

Explore configurations of collection electrode, and pixel size

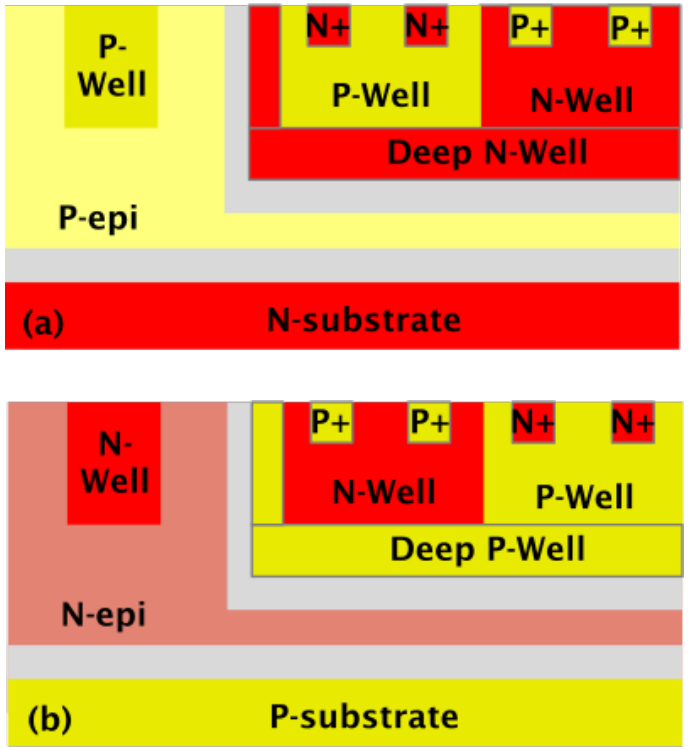


Starting point:

ALICE ITS **ALPIDE** chip

TowerJazz: Recap from July meeting

- **Junction on the backside** to increase depletion region
- **RAL-TJ** approach
- Two options: a) invert substrate or b) invert epitaxial layer with respect to standard TJ process
- Option a) prototyped in the context of the **ATLAS ITK strip detector**
- Option b) proposed by us in the context of a **STFC funded PRD** (Birmingham, RAL, Sussex) to exploit the benefit of using an n-type collection electrode



TowerJazz: Update

- Measurement on prototypes with **option a)** revealed that more work on the process is needed to develop backside junction – not possible with the resources available with the DECAL-PRD

- Instead, work toward the DECAL-PRD will investigate using the **standard TJ process** but with **multiple collection electrodes** in the pixel to improve charge collection by drift

- Pixel size will be 60 x 60 μm^2. Smaller pixels may be included as test structures, space permitting

- Expect submission in May 2017

TowerJazz: CERN-TJ modified process

- Recent **CERN-TJ** development
- Planar deep junction – n-type layer above the p-type epitaxial layer – depletion now extends below the deep p-well
- **Investigator chip** tested by **ATLAS & CLIC** groups at CERN
- Preliminary results demonstrate **very fast and full charge collection** – improvements from **enhanced (possibly full) depletion** compared to standard TJ process

1. L. Musa, ALICE ITS, ECFA HL-LHC Experiments Workshop 2016
2. C. Riegel et al., http://dx.doi.org/10.1088/1748-0221/12/01/C01015

TowerJazz: CERN-TJ modified process

- We are preparing to test the investigator chip
  - More than 100 pixel matrices (10x10 pixels)
  - Pixel size: 20x20 to 50x50 μm^2
  - Different size of electrodes
  - **Very good test vehicle for EIC related investigations**

- Possibility of implementing test structures in a submission led by the ATLAS CERN group in late January/early February

- Investigation of **multiple collection electrodes** could also be of interest – as in RAL-TJ option – discussion on-going with CERN

LFoundry: Update

- Access through membership of **RD50 collaboration**

- Submission of different pixel matrices and test structures to LFoundry is scheduled for late spring
  - More than 10 institutes participating

- Preliminary macro-layout defined / design work starting
  - https://indico.cern.ch/event/580875/contributions/2372582/attachments/1374672/2086818/2016_Vilella_RD50_submission_v2.pdf
  - **Active pixel matrices** (timing, imaging, multi-purpose)
  - **Passive test structures** (capacitance measurements, TCT, different pixel sizes and geometry)
  - Aim to achieve the **smallest possible pixel size** (for some options down to 20 x 20 μm^2)

WP1: Status

- Since July we have been working on defining test structures suitable for EIC investigations in both TJ and LF submissions (accessed through existing R&D projects)

- Access to the CERN-TJ investigator chip with improved depletion region compared to ALPIDE will allow study of charge collection as a function of pixel size and pixel geometry

- More submissions with TJ coming later this year investigating the use of multiple collection electrodes, one with the standard process (RAL-TJ) in May and possibly one with the modified process (CERN-TJ) in February

- A prototype including active and passive test structures covering a large range of flavours in terms of functionality, pixel size and testability are defined for the RD50 submission investigating LFoundry technology

WP2: Simulations

- Plan for new postdoc to work on simulations and sensor tests
  - 50% funded through EIC R&D funds

- Awaiting contract from BNL
  - Process started in November, submitted to BNL in December
  - Have pre-approval to create new post
  - Identified a candidate to fill the post
  - Hopeful for a February start date

- Additional funding requests
  - Applied for matching funds through our STFC consolidated grant
  - Possibility to apply for STFC project R&D funds

eRD18: Project summary

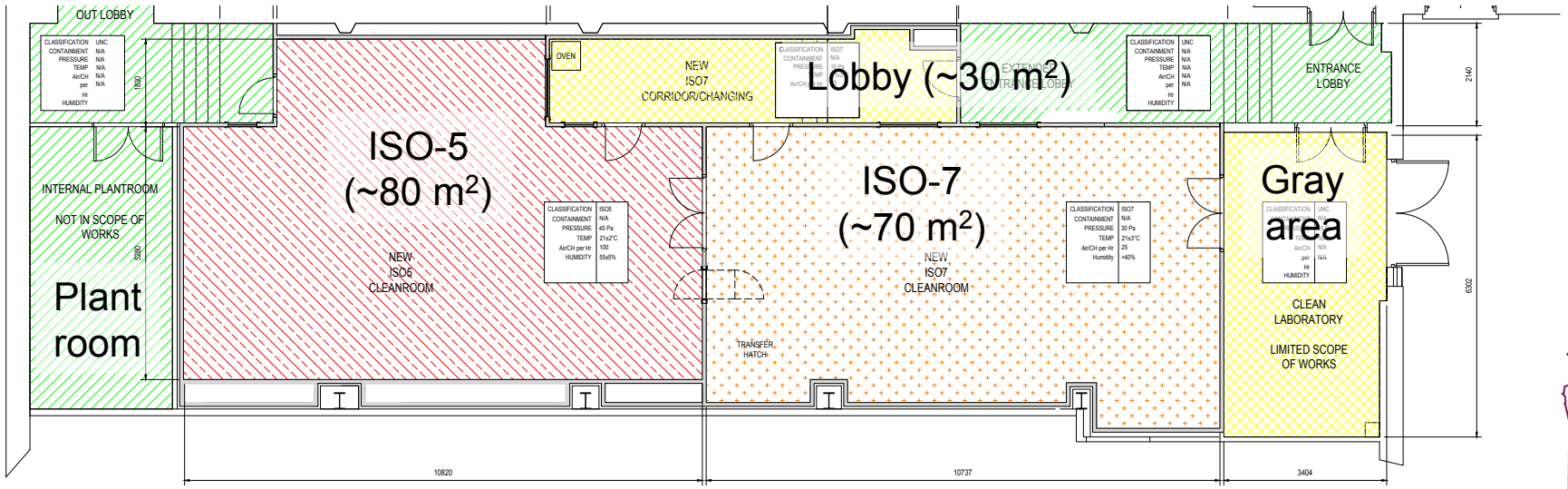
- WP1: Sensor development
  - Exploring RAL-TJ option with multiple electrodes for charge collection
  - CERN-TJ developments provide new opportunities
  - Preparing to test the CERN-TJ investigator chip
  - Plan to investigate test structures with EIC flavour
  - LFoundry submission under preparation

- WP2: Simulations
  - Expect new postdoc to start soon with EIC funding
  - Candidate identified to fill the post
  - Additional funding requests made and planned
  - Expect first results by the next meeting

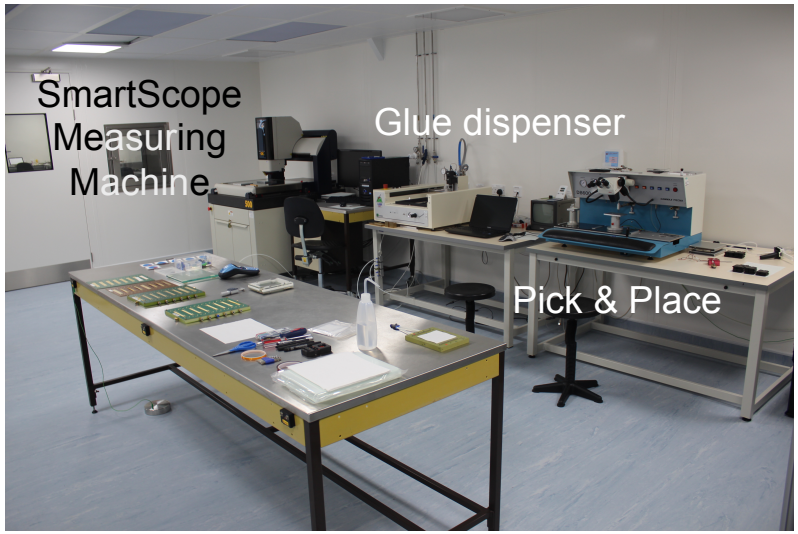
Back-up

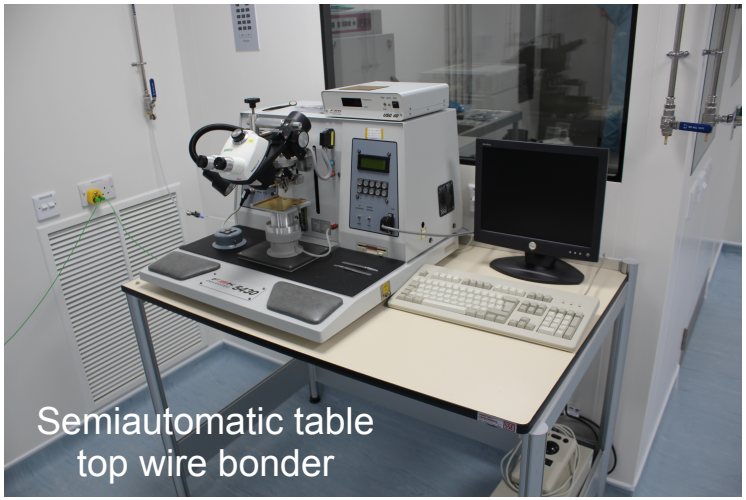
Instrumentation at University of Birmingham

- ATLAS SCT and ITK strips (Phase II upgrade)
- New Instrumentation Laboratory: **Birmingham Instrumentation Laboratory for Particle physics and Applications (BILPA)**
  - Investment in new ~180 m^2 laboratory; available from July 2016
  - New academic appointments: Phil Allport, Laura Gonella, Steve Worm
  - Expanding **manufacturing capability** and growing **new R&D in MAPS**

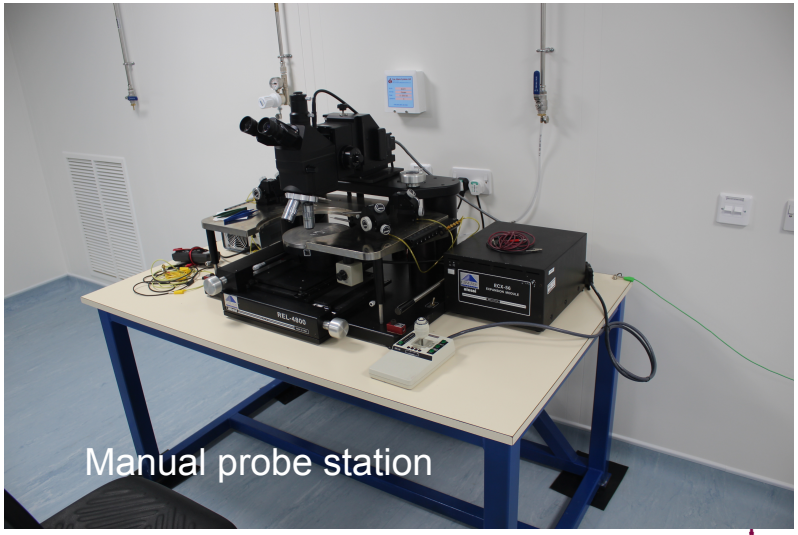


BILPA – ISO5 room





BILPA



Coming soon:
Semi-automatic probe station
TCT Laser system