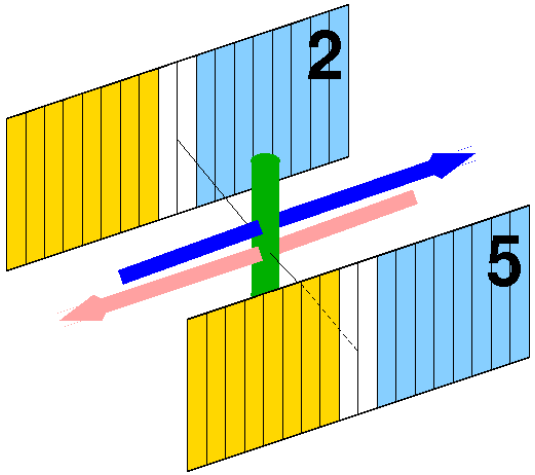
A. Poblaguev

# *VME based DAQ for the Hjet (status report)*

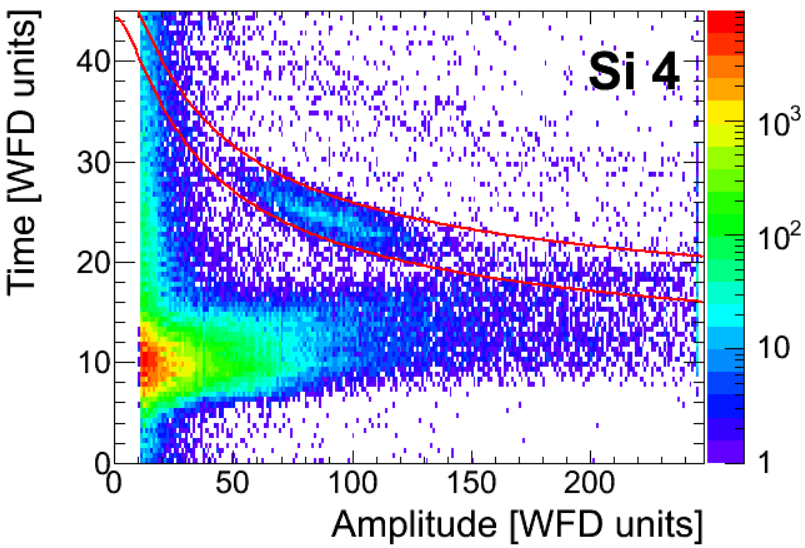
# *H-Jet Polarimeter at RHIC*

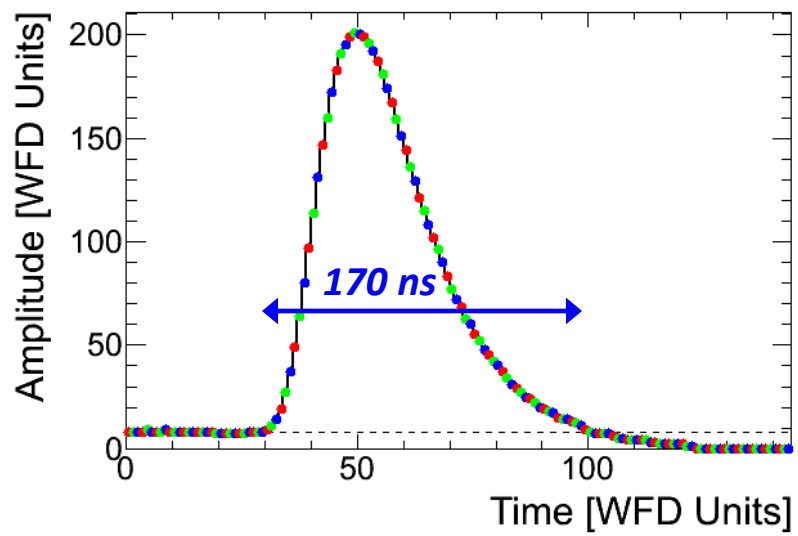



**Measure recoil proton rate in 96 Si strips**

- No signal correlation between strips
- Average rate **6 Hz** per strip
- Signals have to be measured with high (>0.999) efficiency

**Beam bunch frequency** 9.38 MHz (106.5 ns)
**DAQ is based on CAMAC WFD** (8 bit, 420 MHz)



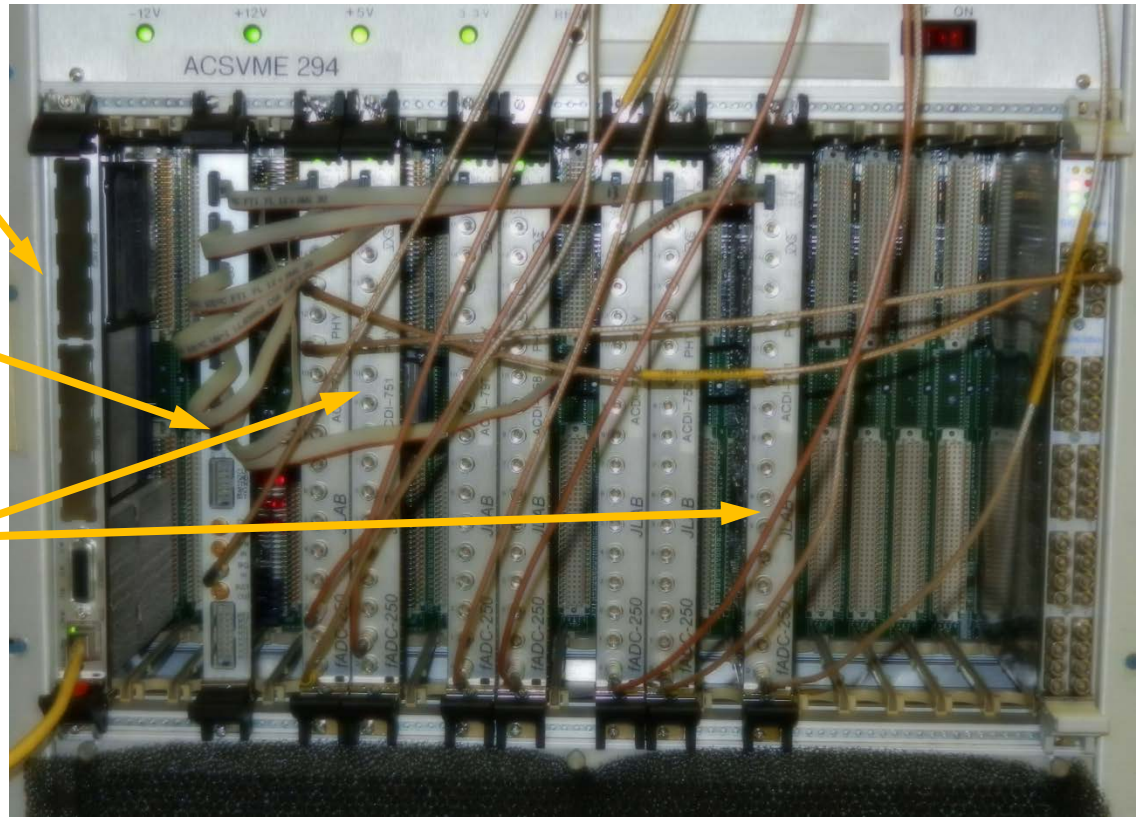
# *Upgrade of the H-Jet DAQ (VME based)*

- **VME64x crate**
- **SBC VX 915/11-14 (Concurrent Technologies)**
- **6+1 FADC 250 (borrowed at Jlab)**
- **1 SDC (borrowed at Jlab)**

***SBC***
(single board computer)

***SDC***
**(signal distribution card)**

***FADC250***
(250 MHz Flash ADC)

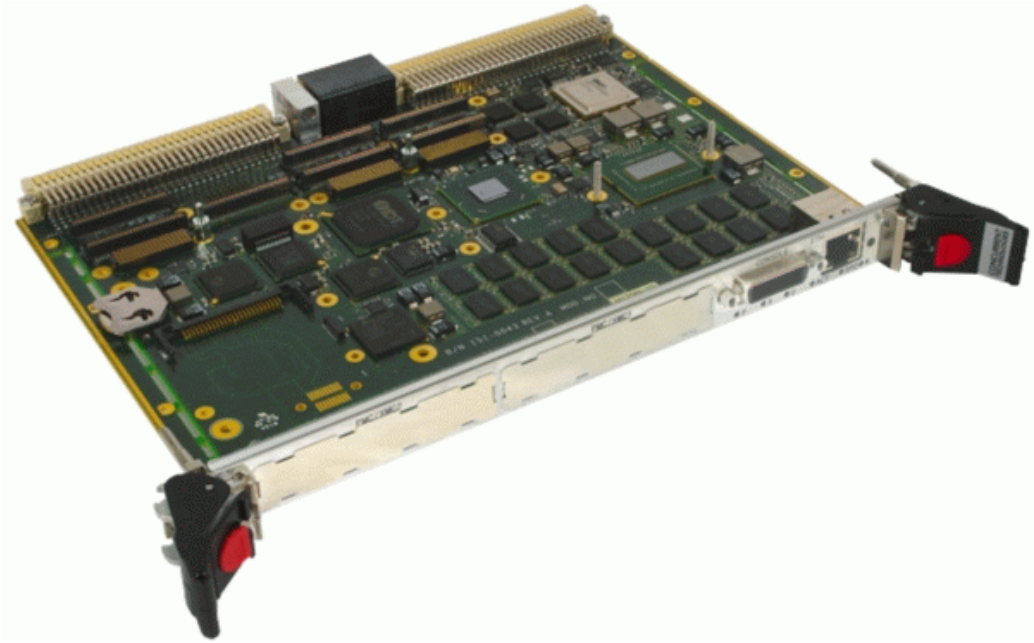


# *Single Board Computer (SBC)*

CONCURRENT TECHNOLOGIES

**VX 915/011-14**

- 4-core 2.1 GHz Intel Core i7-3612QE Processor
- 16 Gbytes DDR3-1600 DRAM with ECC
- VME64 interface supporting A64/A32/A24/A16/D64/D32/D16/D8(E0), MBLT64, 2eSST and 2eVME
- 500 Gbyte Hard Drive
- Red Hat Enterprise 6 Linux



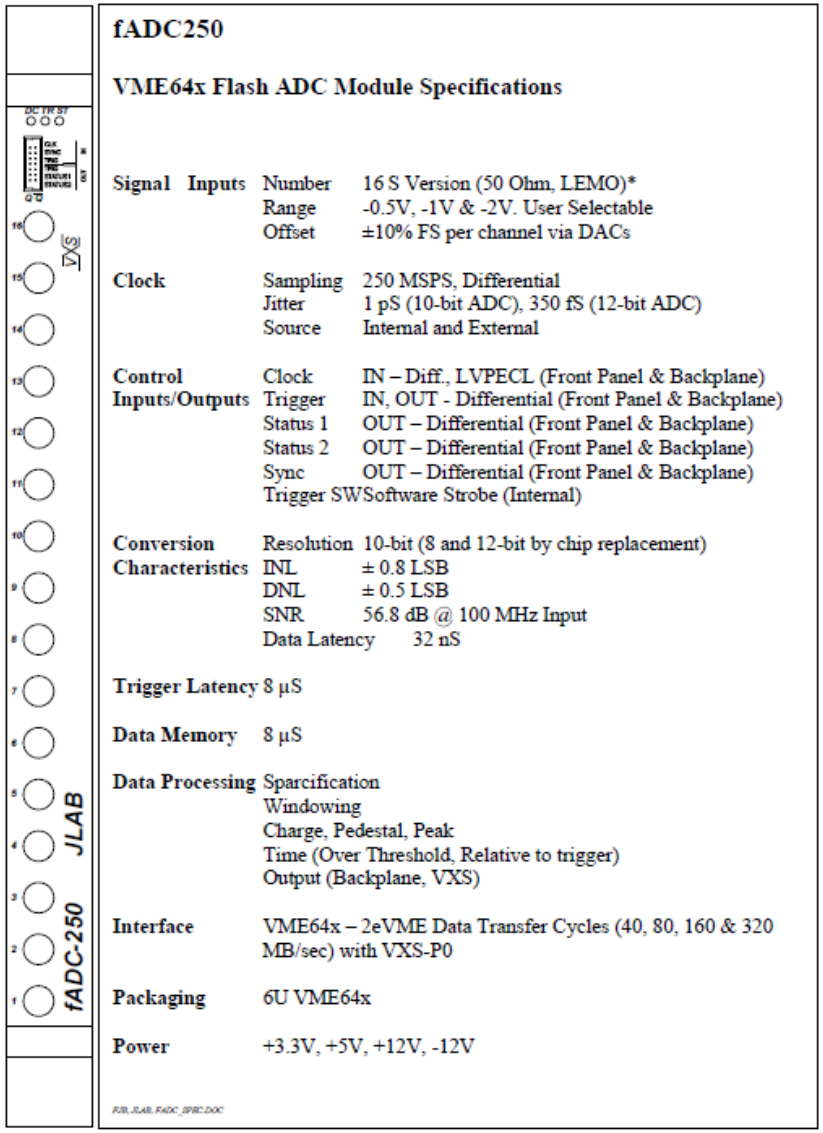
# *Signal Distribution Card (SDC)*

***The board was designed for the Jlab Hall D.***

- ***The SDC distributes synchronized Clock, Trigger, and Sync Reset signals to up to 7 FADC boards.***
- ***Supports external and internally generated signals***

# FADC250

***The board was designed for the Jlab Hall D.***



**fADC250**

**VME64x Flash ADC Module Specifications**

| | | |
|---|---|---|
| **Signal Inputs** | Number | 16 S Version (50 Ohm, LEMO)* |
| | Range | -0.5V, -1V & -2V. User Selectable |
| | Offset | ±10% FS per channel via DACs |
| **Clock** | Sampling | 250 MSPS, Differential |
| | Jitter | 1 pS (10-bit ADC), 350 fS (12-bit ADC) |
| | Source | Internal and External |
| **Control Inputs/Outputs** | Clock | IN – Diff., LVPECL (Front Panel & Backplane) |
| | Trigger | IN, OUT - Differential (Front Panel & Backplane) |
| | Status 1 | OUT – Differential (Front Panel & Backplane) |
| | Status 2 | OUT – Differential (Front Panel & Backplane) |
| | Sync | OUT – Differential (Front Panel & Backplane) |
| | Trigger SW | Software Strobe (Internal) |
| **Conversion Characteristics** | Resolution | 10-bit (8 and 12-bit by chip replacement) |
| | INL | ± 0.8 LSB |
| | DNL | ± 0.5 LSB |
| | SNR | 56.8 dB @ 100 MHz Input |
| | Data Latency | 32 nS |
| **Trigger Latency** | 8 µS | |
| **Data Memory** | 8 µS | |
| **Data Processing** | Sparcification<br>Windowing<br>Charge, Pedestal, Peak<br>Time (Over Threshold, Relative to trigger)<br>Output (Backplane, VXS) | |
| **Interface** | VME64x – 2eVME Data Transfer Cycles (40, 80, 160 & 320 MB/sec) with VXS-P0 | |
| **Packaging** | 6U VME64x | |
| **Power** | +3.3V, +5V, +12V, -12V | |

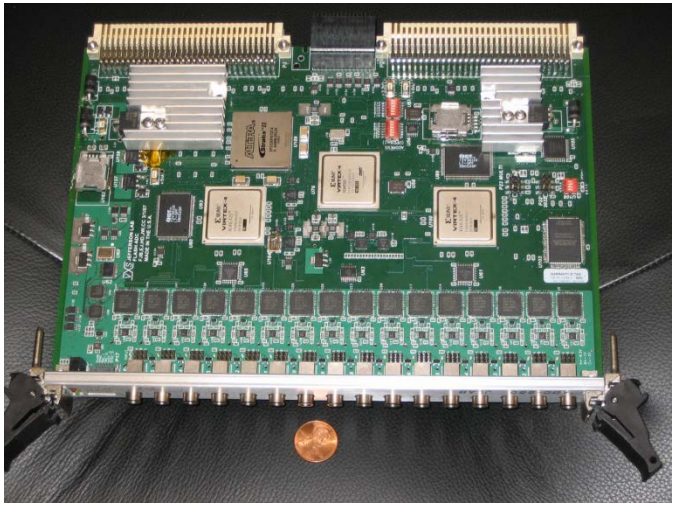


- ***250 MHz***
- ***16 Channel***
- ***Internal Trigger (not available yet!)***
- ***Waveform length up to 511 samples (2 us)***
- ***Dead Time Free***

**External Inputs:**

(from the Signal Distribution Card)

- ***Trigger***
- ***Sync Reset***
- ***Clocks***



# *Basic requirements for the H-Jet WFD*

**We need dead time free system: signal (1 MeV) detection efficiency > 0.999**

**Expected rates (upper limit)**

| | Triggers ( Hz) | Data (kByte/sec) |
|---|---|---|
| Channel | 20 | 4 |
| Board | 300 | 60 |
| Crate | 2000 | 400 |

***For estimates we use a factor 3 higher rates than in existing CAMAC DAQ to account the increased size of new Si detectors and a possible lower threshold.***

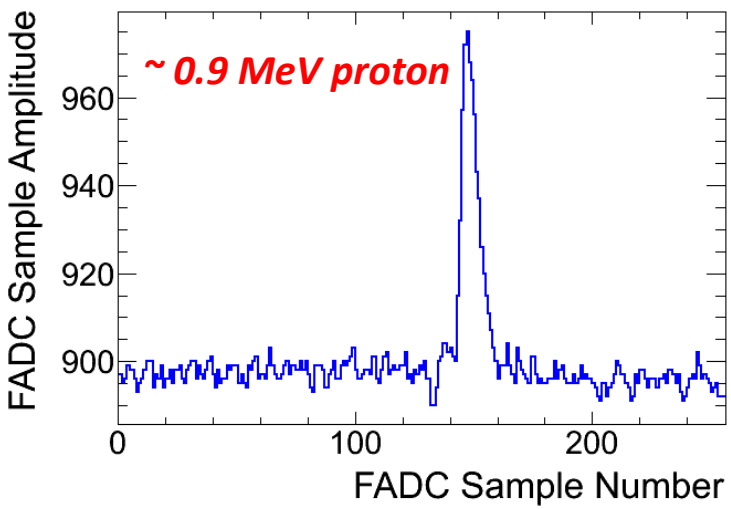
- ***Expected signal rates are very moderate for the VME system***
  ***→ we can use a standard firmware.***
- ***Internal trigger capability is required***
- ***4 ns sampling is sufficient for the H-Jet signals***

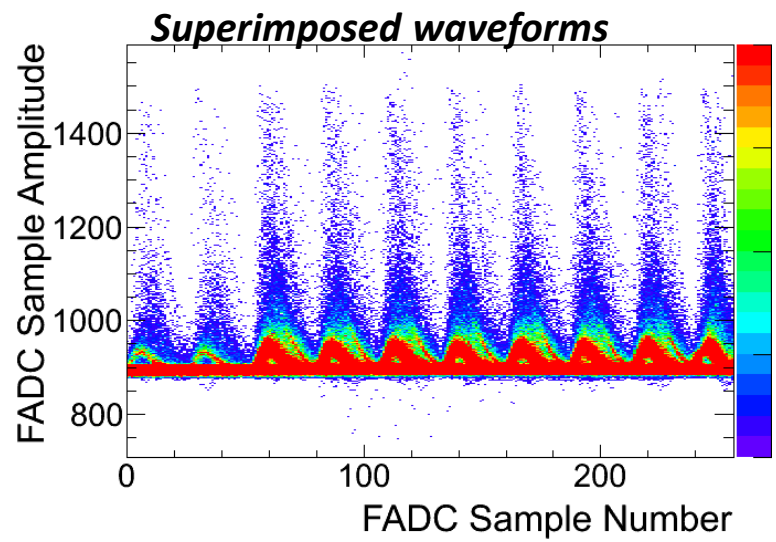
# H-Jet. Tests of FADC250 (March 1012)

***Trigger:*** ***BunchZero coincidence with Signal 1 or 2***
***(not synchronized with clocks)***

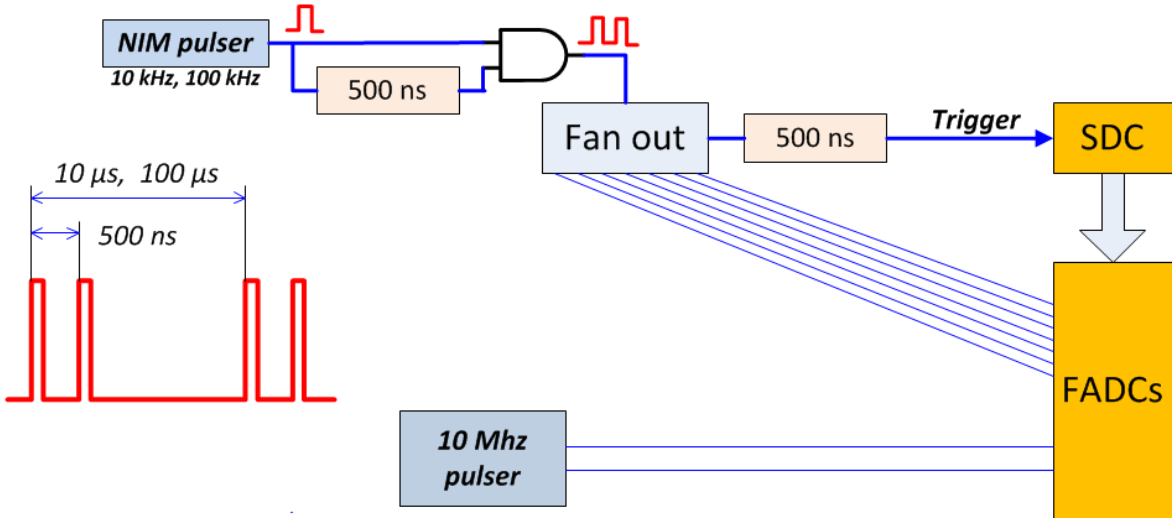
***Inputs:*** ***0. BunchZero***
***1. Signal 1 (not amplified in shaper)***
***2. Signal 2 (not amplified in shaper)***

***Data:*** ***256 samples for every input***



# New Tests of the FADC250




***Tests have been done with external triggers***

***Works well:***

- *200 kHz trigger, 1 entry signal PTW=100*
- *20 kHz trigger, 10 entry signals, PTW=100*
- *100 Mbyte/sec readout is easily achievable.*

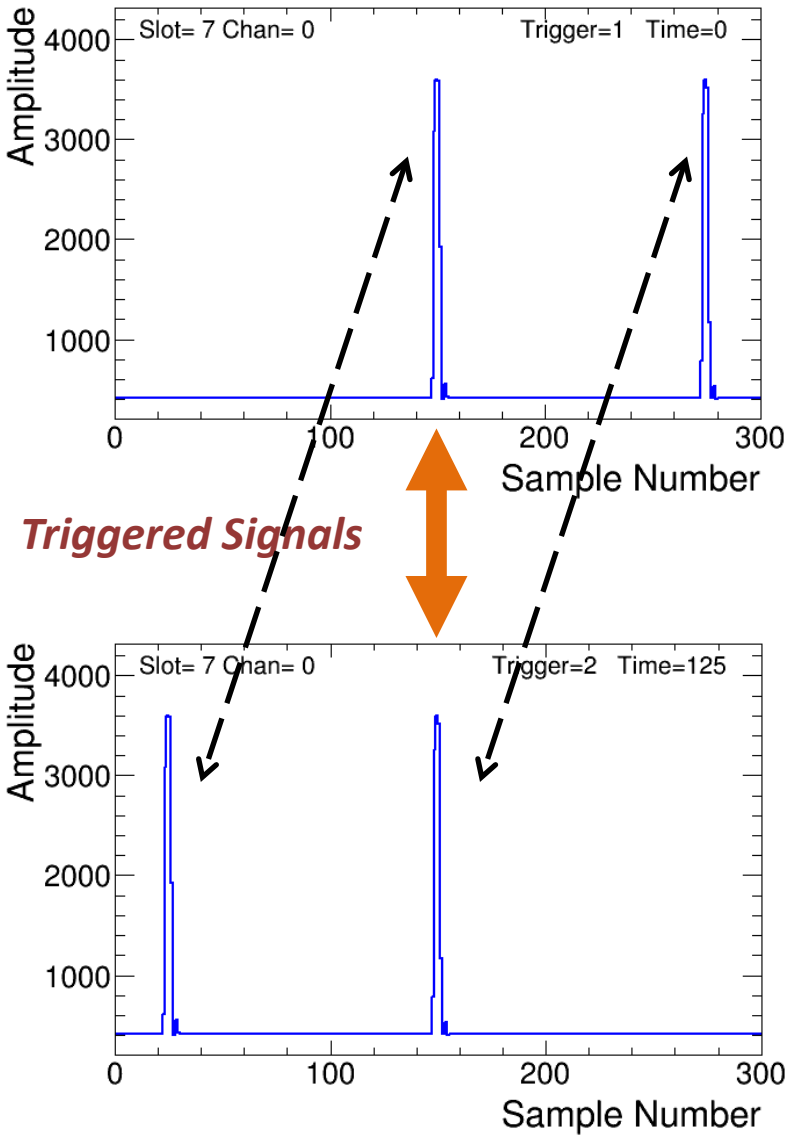
***Not dead time free:***

- *10 MHz trigger, PTW=100 (accepts 8 events)*
- *1 MHz trigger, PTW=50 (accepts 380 events)*
- *1 MHz trigger, PTW=250 (accepts 40 events)*

*** PTW is number of samples per waveform**

***No problems with an expeted FADC performance in the Hjet DAQ are seen at the moment.***

# *Test of the dead time free capability*




- ***Time between triggers 500 ns***
- ***The same signals are seen in different events***

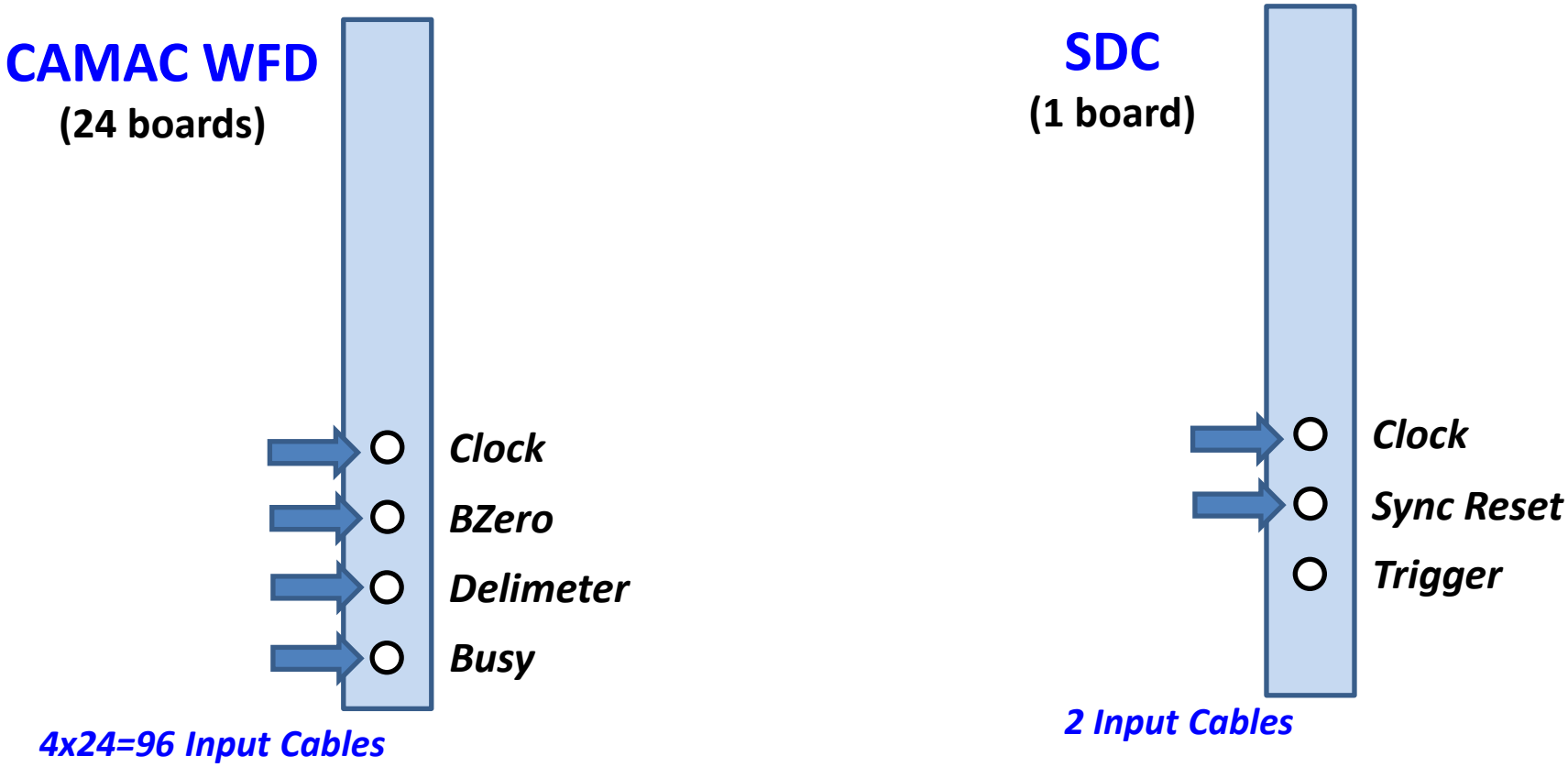
# *Clocks*

**External Clock for WFD is derived from the RF frequency 28.15 MHz**

| | | | |
|---|---|---|---|
| Existing freq. | **140.75 MHz** | (x 5) | 15x3 samples/bunch |
| Considered: | 225.20 MHz | (x 8) | 24 samples /bunch |
| | **243.97 MHz** | (x $8^2/_3$) | 26 samples/bunch |
| | 250.02 MHz | (x $8^8/_9$) | 80 samples/ 3 bunch |

- ***A custom (BNL made) modules are used for frequency multiplication and fan-out at H-Jet***
- ***A chip used for multiplication limits the output frequency by 250 MHz.***
- ***Not tested yet for the new DAQ.***

# *WFD Control Signals*




- ***For the H-Jet we do not really need Delimeter and Busy inputs***
- ***Already available BZero signal should be used as Sync Reset. Actually we need only one signal per RHIC fill.***
- ***New DAQ may be assembled without destroying old system (except for relocation of 96 signal cables)***

# *DAQ Control Signals*

***The HJet DAQ is employing 3 external electrical signal to control the operation:***

- **VETO**
- **Up**
- **Down**

***The signals are delivered through a CAMAC Input Register***

***We need these signals in the new VME based DAQ:***

- ***VME Input register ? Could be found in BNL but signal level conversion is needed.***
- ***CPU COM port (Igor)***
- ***The 7$^{th}$ (spare) FADC can be used to detect these signals***

# *External Triggers*

***For special studies (e.g. baseline study) we may want to use prescale RF signal as external trigger.***

- ***A VME prescale board ?***
- ***Perhaps, the V124 (which distributes the RF signals) could be used for that purpose. Has to be checked with Control Group.***

# *A "spy" DAQ for the pCarbon.*

- ***The pCarbon shapers utilize only 12 channels of 16.***
- ***Every 4$^{th}$ channel may be spied (before shaping)***

***Up to 18 pCarbon Channels may be directed (after some modification of the shapers) to the spare FADC.***

**<u>The main goals:</u>**

- Study of the possible FADC250 performance in the pCarbon polarimeter.
- Study RF noise in the pCarbon detectors
- Study possible calibration methods in the pCarbon
- An independent monitoring of the pCarbon polarimeter.

# *General Comments*

- ***At moment I am naively optimistic about readiness of the new VME based DAQ for the Run15.***
- ***Internal Trigger Capability is not yet available (A help from Jlab is needed)***
- ***We are using unique (not available around) devices such as VME64x crate and SBC. We have no a substitute in case of failure.***
- ***Old CAMAC DAQ must be kept operational.***
- ***New DAQ software should be compatible with old one:***
  - ***User Interface should be the same***
  - ***There should be a conversion from new data format compatible with the old format.***

# *Outline*

- ***The software to work with FADC250 and SDC is mainly ready***
- ***The software is ready for the tests of new Si detectors (Bldg. 930, alpha-source)***
- ***After the tests the VME crate will move to the Hjet counting room at Bldg. 1012 and building of the new DAQ will be started.***
- ***Preparation of the software for new DAQ will start shortly.***

- ***Some technical problems still should be resolved.***