

WFD Version 10 as on March 23, 2005

Note: * denotes new features of V10 compared to V9

Command Summary

Function	R/W	Bits	Words	Description
Board Functions				
F0A8/F16A8	RW	16	1	Read/Write Board Control Register (BCR)
F0A9/F16A9	RW	16	1	Read/Write Xilinx Select Register (XSR)
F0A10/F16A10	RW	16	1	Read/Write JTAG Control Register (JCR)
F16A12	W	16	1	Write Data to memory
Channel Functions				
*F0A0, F1/F17A7				Dummy, no function
F0A1	R	24	1536	Read Histograms
*F0A2	R	8	1	Read Baseline
F0A3	R	24	16	Read Special Scalers
F1A0/F17A0	RW	16	512	Read/Write LUT
F1A1/F17A1	RW	24	1	Read/Wrire CSR
F1A2/F17A2	RW	16	1	Read/Write Trg
F1A3/F17A3	RW	16	1	Read/Write Win
*F1A4/F17A4	RW	16	1	Read/Write Dly
F1A5/F17A5	RW	16	16	Read/Write Bunch Pattern
F1A6	R	16	1	Read Delimiter Counter
F8A1				Copy Histograms to Memory
F9A0				Global reset
F9A1				Reset Scalers and Histograms
F9A2				Reset Address Pointers, Empty FIFOs
F9A3				Reset Revolution Counter
F9A6				Reset Delimiter Counter
Memory Controller Functions				
F0A0	R	16	49/4	Read Data from Memory
F0A1	RW	16	1	Read/Write Memory Controller CSR (MCSR)
F1A0/F17A0	RW	16	1	Read/Write Memory Pointer Lo16 (do this first)
F1A1/F17A1	RW	16	1	Read/Write Memory Pointer Hi16

BCR Summary (F0A8/F16A8, 16 bit)

Bit	R/W	Description
0	RW	Clock Select
1	R	0 – Reserved
2	RW	JTAG Select
3	W	Pulse 'PROG'
7:4	RW	BunchZ Delay
11:8	RW	Same Words to memory
14:12	R	0 – Reserved
15	R	'DONE' Status

CSR Summary (F1A1/F17A1, 24 bit)

Bit	R/W	Description
*0:1	RW	Mode
3:2	RW	Integral Divider
4	RW	Enable Transfer to Memory
5	RW	Fine Histogram Mode
7:6	RW	Channel Number
*8	RW	CFD Threshold 0.5 (0) / 0.25 (1). In V9, this bit controlled 3-pt filter, which is always ON in V10.
*9	RW	Disable all delimiters
10	RW	Enable 120-bunch Mode
*11	RW	Enable trigger window for 'JET' mode
12	RW	Enable Rectangular Lookup
13	RW	Enable Internal Revolution Delimiter
14	R	Histogram to Memory Active
15	RW	Software Delimiter/Delimiter Pending
*16	R	0 – Reserved
17	R	Histogram Reset Active
18	R	Integral Overflow
19	R	Scaler/Hisogram Overflow
20	R	No Inhibit
23:21	R	0 – Reserved

Front Panel Summary

Name	Func.	Std.	Description
TTL A	Output	'LVTTL'	140 MHz monitor
TTL B	Output	'LVTTL'	Unused
TTL C	Output	'LVTTL'	Bunch, 15 CLK period, 1 CLK length, synchronized with Delayed Bunch Zero
TTL D	Output	'LVTTL'	Delayed Bunch Zero Monitor, 1800 CLK period, 1 CLK length
ACLK	Input	C-Decoupled	External 140 MhZ Clock. ± 0.2 V is enough.
NIM B	Input	NIM	External Delimiter (GCC)
NIM C	Input	NIM	External Inhibit
NIM D	Input	NIM	External Bunch Zero
CH A	Input	Analog	Channel 0 analog input. ≈ 250 mV full scale.
CH B	Input	Analog	Channel 1 analog input
CH C	Input	Analog	Channel 2 analog input
CH D	Input	Analog	Channel 3 analog input
Offset	Jumper		Must be set to 'YES' position for negative signals
Offset	VarR		Baseline adjustment. Good number is 240 ampl. units for negative signals

Note: So called 'LVTTL' is 100 Ohm source terminated 3 V TTL output, making only 1 V on 50 Ohm load.

Func.	Description	Condition																														
Board Functions A8-A9																																
Z,C	General Reset to the board and all channels																															
I	CAMAC Inhibit is ORed with the front panel Inhibit and is used for the blocking of data streams in all modes. The resulting Inhibit is internally synchronized with BunchZ signal.																															
F0A8 F16A8 (16)	Read/Write Board Control Register (BCR): <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Bit</th> <th></th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>R/W</td> <td>Board Clock Select (CAMAC interface is always clocked internally): 1 – External clocks from ACLK front panel input 0 – Internal 70 MHz clocks from crystal oscillator</td> </tr> <tr> <td>1</td> <td>R</td> <td>0 – Reserved</td> </tr> <tr> <td>2</td> <td>R/W</td> <td>Xilinx Chain JTAG select: 1 – JTAG controlled by CAMAC F0A10/F16A10 0 – JTAG repeated from/to back panel connector</td> </tr> <tr> <td>3</td> <td>W</td> <td>1 – Pulse Xilinx 'PROG' – initiate Xilinx configuration from FLASH EEPROM</td> </tr> <tr> <td>7:4</td> <td>R/W</td> <td>Delay of front panel BunchZ to channels in terms of 70 MHz clocks (=12 time units). 2 CLK are always added.</td> </tr> <tr> <td>11:8</td> <td>R/W</td> <td>Number of the same words to be transferred to the Memory Controller with F16A12</td> </tr> <tr> <td>14:12</td> <td>R</td> <td>0 – Reserved</td> </tr> <tr> <td>15</td> <td>R</td> <td>Xilinx 'DONE' status: 1 – 'DONE'</td> </tr> <tr> <td>23:16</td> <td>R</td> <td>0 – Not used</td> </tr> </tbody> </table>	Bit		Description	0	R/W	Board Clock Select (CAMAC interface is always clocked internally): 1 – External clocks from ACLK front panel input 0 – Internal 70 MHz clocks from crystal oscillator	1	R	0 – Reserved	2	R/W	Xilinx Chain JTAG select: 1 – JTAG controlled by CAMAC F0A10/F16A10 0 – JTAG repeated from/to back panel connector	3	W	1 – Pulse Xilinx 'PROG' – initiate Xilinx configuration from FLASH EEPROM	7:4	R/W	Delay of front panel BunchZ to channels in terms of 70 MHz clocks (=12 time units). 2 CLK are always added.	11:8	R/W	Number of the same words to be transferred to the Memory Controller with F16A12	14:12	R	0 – Reserved	15	R	Xilinx 'DONE' status: 1 – 'DONE'	23:16	R	0 – Not used	
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F0A9 F16A9 (16)	Read/Write Xilinx Select Register (XSR). <ul style="list-style-type: none"> • On individual channel Write (F16–F23) or Control (F8–F15) functions all channels with corresponding XSR bit set will receive the command and data. • On individual channel Read (F0–F7) functions data will be read from the channel with the lowest number for which the XSR bit is set. <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 10px;"> <thead> <tr> <th>Nw</th> <th>23</th> <th>16</th> <th>15</th> <th>5</th> <th>4</th> <th>3</th> <th>2</th> <th>1</th> <th>0</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>MemCntr</td> <td>Ch3</td> <td>Ch2</td> <td>Ch1</td> <td>Ch0</td> </tr> </tbody> </table>	Nw	23	16	15	5	4	3	2	1	0	0	0	0	0	0	MemCntr	Ch3	Ch2	Ch1	Ch0											
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*FOA2 (8)	<p>Read current Baseline Average values. Mainly intended for test purposes. As the values are constantly changing and no latching is provided, there is no guarantee that the reading is always absolutely correct. Compared to V9, only R channel is used for the baseline calculations, since the 3-pt filter makes effective baseline alignment between channels and the value itself is only used to shift the signal to the level of 8.</p> <table border="1"> <thead> <tr> <th>Nw</th> <th>23</th> <th>16</th> <th>15</th> <th>8</th> <th>7</th> <th>0</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td></td> <td>0</td> <td></td> <td></td> <td>Mean0[7:0](R)</td> </tr> </tbody> </table>	Nw	23	16	15	8	7	0	0	0		0			Mean0[7:0](R)																																				
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F0A3 (24)	<p>Read Special Scalers: 16 words in pairs (Lo,Hi) represent values of 8 32-bit scalers. Bits [19:16] of each word are the word number in the sequence. The current contents of all of the sclaers is latched on the reading of the Lo part of the first scaler, so that even while scaling is in progress, the values correspond to a single moment of time. Words 10–15 are not used, but must be read out to complete the sequence.</p> <table border="1"> <thead> <tr> <th>Nw</th> <th>23</th> <th>20</th> <th>19</th> <th>16</th> <th>15</th> <th>0</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td colspan="3">+Pol bunches through both cuts, [15:0]</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td colspan="4">Same, [31:16]</td> </tr> <tr> <td>2</td> <td>0</td> <td>2</td> <td colspan="4">–Pol bunches through both cuts, [15:0]</td> </tr> <tr> <td>3</td> <td>0</td> <td>3</td> <td colspan="4">Same, [31:16]</td> </tr> <tr> <td>4</td> <td>0</td> <td>4</td> <td colspan="4">0-Pol bunches through both cuts, [15:0]</td> </tr> <tr> <td>5</td> <td>0</td> <td>5</td> <td colspan="4">Same, [31:16]</td> </tr> <tr> <td>6</td> <td>0</td> <td>6</td> <td colspan="4">Filled bunches through AT cut, Int<LL, [15:0]</td> </tr> <tr> <td>7</td> <td>0</td> <td>7</td> <td colspan="4">Same, [31:16]</td> </tr> <tr> <td>8</td> <td>0</td> <td>8</td> <td colspan="4">Filled bunches through AT cut, Int>UL, [15:0]</td> </tr> <tr> <td>9</td> <td>0</td> <td>9</td> <td colspan="4">Same, [31:16]</td> </tr> <tr> <td>10</td> <td>0</td> <td>10</td> <td colspan="4">0</td> </tr> <tr> <td>...</td> <td>0</td> <td>...</td> <td colspan="4">0</td> </tr> <tr> <td>15</td> <td>0</td> <td>15</td> <td colspan="4">0</td> </tr> </tbody> </table>	Nw	23	20	19	16	15	0	0	0	0	0	+Pol bunches through both cuts, [15:0]			1	0	1	Same, [31:16]				2	0	2	–Pol bunches through both cuts, [15:0]				3	0	3	Same, [31:16]				4	0	4	0-Pol bunches through both cuts, [15:0]				5	0	5	Same, [31:16]				6	0	6	Filled bunches through AT cut, Int<LL, [15:0]				7	0	7	Same, [31:16]				8	0	8	Filled bunches through AT cut, Int>UL, [15:0]				9	0	9	Same, [31:16]				10	0	10	0				...	0	...	0				15	0	15	0				CSR[1:0]=2 or CSR[1:0]=3
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F1A0 F17A0 (16)	<p>Read/Write LookUp Tables (LUT), 512 words: Words 0:255 represent limits for Time(Amplitude) lookup table, Lo byte – the lower limit for Time at the given Amplitude, Hi byte – the upper limit. Words 256:511 are the limits for the Integral(Amplitude) lookup table in the same manner.</p> <table border="1"> <thead> <tr> <th>Nw</th> <th>23</th> <th>16</th> <th>15</th> <th>8</th> <th>7</th> <th>0</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td colspan="2">T UL if A=0 [7:0]</td> <td colspan="2">T LL if A=0 [7:0]</td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td colspan="2">T UL if A=1 [7:0]</td> <td colspan="2">T LL if A=1 [7:0]</td> <td></td> </tr> <tr> <td></td> <td></td> <td colspan="5">...</td> </tr> <tr> <td>255</td> <td>0</td> <td colspan="2">T UL if A=255 [7:0]</td> <td colspan="2">T LL if A=255 [7:0]</td> <td></td> </tr> <tr> <td>256</td> <td>0</td> <td colspan="2">I UL if A=0 [7:0]</td> <td colspan="2">I LL if A=0 [7:0]</td> <td></td> </tr> <tr> <td></td> <td></td> <td colspan="5">...</td> </tr> <tr> <td>511</td> <td>0</td> <td colspan="2">I UL if A=255 [7:0]</td> <td colspan="2">I LL if A=255 [7:0]</td> <td></td> </tr> </tbody> </table> <p>Note: An event is considered to be good if the given parameter is strictly greater than AND strictly lower than the corresponding limit, so that values of Time and Integral 0 and 255 are always forbidden.</p>	Nw	23	16	15	8	7	0	0	0	T UL if A=0 [7:0]		T LL if A=0 [7:0]			1	0	T UL if A=1 [7:0]		T LL if A=1 [7:0]					...					255	0	T UL if A=255 [7:0]		T LL if A=255 [7:0]			256	0	I UL if A=0 [7:0]		I LL if A=0 [7:0]					...					511	0	I UL if A=255 [7:0]		I LL if A=255 [7:0]																																													
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Func.	Description		Condition
F1A1 (24) F17A1 (16)	Read/Write Control and Status Register (CSR):		
	*0:1	R/W	Mode of operation: 0 – Dummy, no signals are stored or processed. 1 – 'JET' , long waveform with baseline subtraction and signal inversion, threshold trigger position within the current bunch, +B#/R#. The waveform record length and its portion length before the trigger is defined by the value of the Dly register. 2 – 'AT' , Ampl/TCFD/Int/TInt/B#/R#, scalers active. 3 – 'ALL' , Same as 2, but the waveform is added before the defined parameters, scalers active.
	3:2	R/W	Integral divider: Calculated integral is divided by $2^{CSR[3:2]+2}$ in order to fit into a 8-bit value.
	4	R/W	1 – Transfer data to memory as soon as it's ready. 0 – Stop the transfer
	5	R/W	1 – Fine 2D histogram 0 – Coarse 2D histogram
	7:6	R/W	0-3 – Channel Number. Should be programmed by the software to have the channel identification in the events stored to memory.
	*8	R/W	1 – CFD threshold is 1/4 of the amplitude 0 – CFD threshold is 1/2 of the amplitude
	*9	R/W	1 – Disable all delimiters (including the software)
	10	R/W	1 – 120 Bunch mode 0 – 60 Bunch mode
	*11	R/W	1 – Threshold trigger in 'JET' mode can only arise in the portion of the bunch period, defined by the Win register 0 – Threshold trigger is sensitive to the signal level independently of the bunch structure.
	12	R/W	1 – In 'AT' or 'ALL' modes, use Rectangular Lookup instead of LUTs for the events going to memory. No effect on scaler/histogram performance.
	13	R/W	1 – Internal delimiter from revolution counter / 2^9 0 – External delimiter from the front panel.
	14	R	1 – Histogram transfer to memory active, should be 1 about 20 μ s after F8A1 (never tested).
	15	W R	1 – Software delimiter (will immediately transfer the delimiter to memory if CSR4=1 and no INH). 1 – Delimiter pending.

Func.	Description	Condition																		
F1A1 F17A1	<p>Control and Status Register (CSR) Contd. :</p> <table border="1"> <tr> <td>*16</td> <td>R</td> <td>– Reserved. Must read 0.</td> </tr> <tr> <td>17</td> <td>R</td> <td>1 during Scaler Reset routine about 20 μs after F9A1.</td> </tr> <tr> <td>18</td> <td>R</td> <td>1 – Integral Overflow: set if the integral $/2^{CSR[3:2]+2}$ exceeds 255.</td> </tr> <tr> <td>19</td> <td>R</td> <td>1 – Scaler Overflow: set if one of the special scalers or histogram bins exceeds 2^{32} or 2^{24} correspondingly.</td> </tr> <tr> <td>20</td> <td>R</td> <td>1 if event selection is not forbidden. Should reflect a NOR of crate INHIBIT and front panel INH.</td> </tr> <tr> <td>23:21</td> <td>R</td> <td>– Reserved. Must read 0.</td> </tr> </table> <p>Note: Overflow bits (CSR18, CSR19) are set once the error occurs and reset by writing new data to CSR.</p>	*16	R	– Reserved. Must read 0.	17	R	1 during Scaler Reset routine about 20 μ s after F9A1.	18	R	1 – Integral Overflow: set if the integral $/2^{CSR[3:2]+2}$ exceeds 255.	19	R	1 – Scaler Overflow: set if one of the special scalers or histogram bins exceeds 2^{32} or 2^{24} correspondingly.	20	R	1 if event selection is not forbidden. Should reflect a NOR of crate INHIBIT and front panel INH.	23:21	R	– Reserved. Must read 0.	
*16	R	– Reserved. Must read 0.																		
17	R	1 during Scaler Reset routine about 20 μ s after F9A1.																		
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23:21	R	– Reserved. Must read 0.																		
F1A2 F17A2 (16)	<p>Read/Write Trigger and low limit Register (Trg):</p> <p>Trg[7:0] – Threshold trigger value in tremes of RAW signal. The baseline value is NOT calculated if the RAW signal has points lower than the Ttg[7:0]. In 'JET' mode the waveform is stored to the FIFO on the same event.</p> <p>Trg[15:8] – Used as low limit in amplitude for:</p> <ul style="list-style-type: none"> • 2D histogram in Fine mode (CSR5=1) • Rectangular lookup window if enabled (CSR12=1) 																			
F1A3 F17A3 (16)	<p>Read/Write Window Register (Win):</p> <p>Win[7:0] – Beginning of the sensitive window from BunchZ, in point frequency units, (1/6 of 70 MHz clock period = 2x time unit). Must never be set to 0. If even 0 is written, the value will be set to 1. Also 2x this value is used as low limit in time for:</p> <ul style="list-style-type: none"> • 2D histogram • Rectangular lookup window if enabled (CSR12=1) <p>Win[15:8] – End of sensitive window, same units. If set to ≥ 90, the window will remain open till the end of the bunch period.</p>																			
*F1A4 F17A4 (16)	<p>Read/Write Delay Register (Dly), only used in 'JET' mode:</p> <p>Dly[7:0] – Total length of the waveform record in 'JET' mode in tremes of 70 MHz periods (6 points each)</p> <p>Dly[15:8] – Number of 70 Mhz periods, recorded prior to the one, containing the first point after the threshold trigger crossing.</p>	CSR[1:0]=1																		

Func.	Description	Condition																																																															
F1A5 F17A5 (16)	<p>Read/Write Bunch Pattern, 16 words. Two bits +Bn and -Bn are used to designate bunch polarity:</p> <table border="1"> <thead> <tr> <th>+Bn</th> <th>-Bn</th> <th>Bunch Signature</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Not Filled</td> </tr> <tr> <td>1</td> <td>0</td> <td>Positive</td> </tr> <tr> <td>0</td> <td>1</td> <td>Negative</td> </tr> <tr> <td>1</td> <td>1</td> <td>Unpolarized</td> </tr> </tbody> </table> <p>The format is:</p> <table border="1"> <thead> <tr> <th>Nw</th> <th>23 16</th> <th>15</th> <th>14 ... 9</th> <th>8</th> <th>7</th> <th>6 ... 1</th> <th>0</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>-B7</td> <td>...</td> <td>-B0</td> <td>+B7</td> <td>...</td> <td>+B0</td> </tr> <tr> <td>1</td> <td>0</td> <td>-B15</td> <td>...</td> <td>-B8</td> <td>+B15</td> <td>...</td> <td>+B8</td> </tr> <tr> <td></td> <td>0</td> <td colspan="6">...</td> </tr> <tr> <td>14</td> <td>0</td> <td>-B119</td> <td>...</td> <td>-B112</td> <td>+B119</td> <td>...</td> <td>+B112</td> </tr> <tr> <td>15</td> <td>0</td> <td colspan="6">X</td> </tr> </tbody> </table>	+Bn	-Bn	Bunch Signature	0	0	Not Filled	1	0	Positive	0	1	Negative	1	1	Unpolarized	Nw	23 16	15	14 ... 9	8	7	6 ... 1	0	0	0	-B7	...	-B0	+B7	...	+B0	1	0	-B15	...	-B8	+B15	...	+B8		0	...						14	0	-B119	...	-B112	+B119	...	+B112	15	0	X						
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1	0	-B15	...	-B8	+B15	...	+B8																																																										
	0	...																																																															
14	0	-B119	...	-B112	+B119	...	+B112																																																										
15	0	X																																																															
F1A6 (16)	Read current Delimiter Counter value.																																																																
*F1A7 F17A7	Dummy, no function																																																																
F8A1	Copy Histograms to memory. CSR14 reflects the status of the operation. Never tested.	CSR4=1																																																															
F9A0	General Reset to the channel: resets all registers, address pointers and register based counters to their initial values, which is usually 0. Does not affect the contents of the histograms.																																																																
F9A1	Reset Scalers: affects both histograms and special scalars. CSR17 reflects the status of the operation.																																																																
F9A2	Reset Address Pointers for all sequential operations such as: histogram and special scalars read, LUT read/write etc. Also resets both FIFOs to the empty state																																																																
F9A3	Reset Revolution Counter. After this operation the counter will start counting revolutions only after the first allowing edge of INH combination.																																																																
F9A6	Reset Delimiter Counter. If the delimiter request is pending, it will also be reset.																																																																

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Memory Controller Functions																																																																																																																																																																																																															
F0A0 F16A0 (16)	<p>Read/Write data from/to memory, increment memory pointer. Q=1 always, so it's the responsibility of the software to keep track of the amount of data in the memory by reading out the pointer after the datastream is stopped. The event formats are:</p> <p>In 'JET' mode: variable number of words per event dependent on the Dly register value ($Nw=3*Dly[7:0]+4$):</p> <table border="1" style="margin-left: 40px;"> <thead> <tr> <th>Nw</th> <th>23</th> <th>16</th> <th>15</th> <th>8</th> <th>7</th> <th>0</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td colspan="5">Channel CSR[15:0]</td> </tr> <tr> <td>1</td> <td>0</td> <td colspan="3">Dly[15:8]</td> <td colspan="2">Dly[7:0]</td> <td></td> </tr> <tr> <td>2</td> <td>0</td> <td colspan="2">Rev#[4:0]</td> <td colspan="2">B#[6:0]</td> <td>TrT[3:0]</td> </tr> <tr> <td>3</td> <td>0</td> <td colspan="5">Revolution#[20:5]</td> </tr> <tr> <td>4</td> <td>0</td> <td colspan="3">Point1[7:0](G)</td> <td colspan="2">Point0[7:0](R)</td> <td></td> </tr> <tr> <td>5</td> <td>0</td> <td colspan="3">Point3[7:0](R)</td> <td colspan="2">Point2[7:0](B)</td> <td></td> </tr> <tr> <td>6</td> <td>0</td> <td colspan="3">Point5[7:0](B)</td> <td colspan="2">Point4[7:0](G)</td> <td></td> </tr> <tr> <td></td> <td></td> <td colspan="5" style="text-align: center;">...</td> <td></td> </tr> </tbody> </table> <p>TrT[3:0] is the number of the 70 MHz period from the bunch start time when the threshold trigger crossing occurred. The bunch number and the revolution number also correspond to this event.</p> <p>In 'AT' mode: 4 words per event:</p> <table border="1" style="margin-left: 40px;"> <thead> <tr> <th>Nw</th> <th>23</th> <th>16</th> <th>15</th> <th>8</th> <th>7</th> <th>0</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td colspan="5">Channel CSR[15:0]</td> </tr> <tr> <td>1</td> <td>0</td> <td colspan="3">CFD Time[7:0]</td> <td colspan="2">Amplitude[7:0]</td> <td></td> </tr> <tr> <td>2</td> <td>0</td> <td colspan="3">Intg Time[7:0]</td> <td colspan="2">Integral[7:0]</td> <td></td> </tr> <tr> <td>3</td> <td>0</td> <td colspan="3">Rev#[8:1]</td> <td colspan="2">R#[0] B#[6:0]</td> <td></td> </tr> </tbody> </table> <p>In 'ALL' mode: 49 words per event:</p> <table border="1" style="margin-left: 40px;"> <thead> <tr> <th>Nw</th> <th>23</th> <th>16</th> <th>15</th> <th>8</th> <th>7</th> <th>0</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td colspan="5">Channel CSR[15:0]</td> </tr> <tr> <td>1</td> <td>0</td> <td colspan="3">Point1[7:0](G)</td> <td colspan="2">Point0[7:0](R)</td> <td></td> </tr> <tr> <td>2</td> <td>0</td> <td colspan="3">Point3[7:0](R)</td> <td colspan="2">Point2[7:0](B)</td> <td></td> </tr> <tr> <td>3</td> <td>0</td> <td colspan="3">Point5[7:0](B)</td> <td colspan="2">Point4[7:0](G)</td> <td></td> </tr> <tr> <td></td> <td></td> <td colspan="5" style="text-align: center;">...</td> <td></td> </tr> <tr> <td>45</td> <td>0</td> <td colspan="3">Point89[7:0](B)</td> <td colspan="2">Point88[7:0](G)</td> <td></td> </tr> <tr> <td>46</td> <td>0</td> <td colspan="3">CFD Time[7:0]</td> <td colspan="2">Amplitude[7:0]</td> <td></td> </tr> <tr> <td>47</td> <td>0</td> <td colspan="3">Intg Time[7:0]</td> <td colspan="2">Integral[7:0]</td> <td></td> </tr> <tr> <td>48</td> <td>0</td> <td colspan="3">Rev#[8:1]</td> <td colspan="2">R#[0] B#[6:0]</td> <td></td> </tr> </tbody> </table> <p>In all modes delimiters may appear in the datastream transferred to memory. The delimiter format is (2 words):</p> <table border="1" style="margin-left: 40px;"> <thead> <tr> <th>Nw</th> <th>23</th> <th>16</th> <th>15</th> <th>8</th> <th>7</th> <th>0</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td colspan="5">Channel CSR[15:0]</td> </tr> <tr> <td>1</td> <td>0</td> <td colspan="5">Delimiter Counter[15:0]</td> </tr> </tbody> </table>	Nw	23	16	15	8	7	0	0	0	Channel CSR[15:0]					1	0	Dly[15:8]			Dly[7:0]			2	0	Rev#[4:0]		B#[6:0]		TrT[3:0]	3	0	Revolution#[20:5]					4	0	Point1[7:0](G)			Point0[7:0](R)			5	0	Point3[7:0](R)			Point2[7:0](B)			6	0	Point5[7:0](B)			Point4[7:0](G)					...						Nw	23	16	15	8	7	0	0	0	Channel CSR[15:0]					1	0	CFD Time[7:0]			Amplitude[7:0]			2	0	Intg Time[7:0]			Integral[7:0]			3	0	Rev#[8:1]			R#[0] B#[6:0]			Nw	23	16	15	8	7	0	0	0	Channel CSR[15:0]					1	0	Point1[7:0](G)			Point0[7:0](R)			2	0	Point3[7:0](R)			Point2[7:0](B)			3	0	Point5[7:0](B)			Point4[7:0](G)					...						45	0	Point89[7:0](B)			Point88[7:0](G)			46	0	CFD Time[7:0]			Amplitude[7:0]			47	0	Intg Time[7:0]			Integral[7:0]			48	0	Rev#[8:1]			R#[0] B#[6:0]			Nw	23	16	15	8	7	0	0	0	Channel CSR[15:0]					1	0	Delimiter Counter[15:0]					<p>CSR[1:0]=1; CSR4=1; MCSR0=1</p> <p>CSR[0:1]=2; CSR4=1; MCSR0=1</p> <p>CSR[1:0]=3; CSR4=1; MCSR0=1</p> <p>CSR[0:1]=1-3; CSR4=1; MCSR0=1</p>
Nw	23	16	15	8	7	0																																																																																																																																																																																																									
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1	0	Dly[15:8]			Dly[7:0]																																																																																																																																																																																																										
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F0A0 F16A0	<p>Contd.</p> <p>If the software issues F8A1 command (never tested), the copy of the channel internal histograms will appear in the memory datastream. The format of the block is (3073 words):</p> <table border="1"> <thead> <tr> <th>Nw</th> <th>23</th> <th>16</th> <th>15</th> <th>8</th> <th>7</th> <th>0</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td colspan="5">Channel CSR[15:0]</td> </tr> <tr> <td>1</td> <td>0</td> <td colspan="5">Bin0 of Bunch# Histo [15:0]</td> </tr> <tr> <td>2</td> <td>0</td> <td>0</td> <td colspan="4">Bin0 of Bunch# Histo [23:16]</td> </tr> <tr> <td>3-240</td> <td>0</td> <td colspan="5">The rest of Bunch# Histo in such pairs</td> </tr> <tr> <td>241-256</td> <td>0</td> <td colspan="5">0</td> </tr> <tr> <td>257-512</td> <td>0</td> <td colspan="5">Amplitude Histo for unpolarized bunches</td> </tr> <tr> <td>513-768</td> <td>0</td> <td colspan="5">Same for positive polarization bunches</td> </tr> <tr> <td>769-1024</td> <td>0</td> <td colspan="5">Same for negative polarization bunches</td> </tr> <tr> <td>1025-3072</td> <td>0</td> <td colspan="5">2D AT Histogram</td> </tr> </tbody> </table> <p>Important Note: The type and size of each block of data is determined by the combination of bits in the first word of the block – CSR[15:0]:</p> <table border="1"> <thead> <tr> <th>CSR15</th> <th>CSR14</th> <th>CSR[1:0]</th> <th>Len</th> <th>Type</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>Must never happen</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>4+Dly[7:0]*3</td> <td>Waveform in 'JET' mode</td> </tr> <tr> <td>0</td> <td>0</td> <td>2</td> <td>4</td> <td>Event parameters in 'AT' mode</td> </tr> <tr> <td>0</td> <td>0</td> <td>3</td> <td>49</td> <td>Wform and pars in 'ALL' mode</td> </tr> <tr> <td>1</td> <td>0</td> <td>X</td> <td>2</td> <td>Delimiter</td> </tr> <tr> <td>0</td> <td>1</td> <td>X</td> <td>3073</td> <td>Histograms</td> </tr> </tbody> </table> <p>Note: The length of the waveform records does not depend on which of the 60/120 bunch modes is selected. In 120 bunch mode the trailing half of the waveform is unused and should read 0.</p>	Nw	23	16	15	8	7	0	0	0	Channel CSR[15:0]					1	0	Bin0 of Bunch# Histo [15:0]					2	0	0	Bin0 of Bunch# Histo [23:16]				3-240	0	The rest of Bunch# Histo in such pairs					241-256	0	0					257-512	0	Amplitude Histo for unpolarized bunches					513-768	0	Same for positive polarization bunches					769-1024	0	Same for negative polarization bunches					1025-3072	0	2D AT Histogram					CSR15	CSR14	CSR[1:0]	Len	Type	0	0	0	0	Must never happen	0	0	1	4+Dly[7:0]*3	Waveform in 'JET' mode	0	0	2	4	Event parameters in 'AT' mode	0	0	3	49	Wform and pars in 'ALL' mode	1	0	X	2	Delimiter	0	1	X	3073	Histograms	CSR4=1; MCSR0=1
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Func.	Description	Condition
F1A0 F1A1 (16)	Read Lo16/Hi16 Memory Address Pointer. The current value of the pointer is latched on F1A0, so that the whole value always corresponds to a single moment of time, and the Lo16 part should be read first.	
F17A0 F17A1 (16)	Write Lo16/Hi16 Memory Address Pointer. The value of the pointer takes effect on F17A1, so the Lo16 part should be written first with F17A0. The new SDRAM page is read to the readout cache on F17A1 if MCSR1=1. Allow $\approx 15\mu s$ for this operation.	

FIFOs

All data streams in channels go through several FIFOs, but since the direct readout of the data is not implemented in V10 and all the data goes to the SDRAM memory as soon as it appears, the depth of the FIFO doesn't matter much. The data needs some buffering only because of the arbitration that takes place between channels for the opportunity to write to SDRAM, and the FIFO depth is enough for that, unless the total data rate acceptable by SDRAM is not too high.

Old and New in V10

1. WFD **V10** uses exactly the same firmware for the Lattice buffer and CamControl chips as **V9**:

- lat_buf10
- lat_tran_10
- lat_clk10_200
- lat_cam10_try1

and exactly the same firmware for the SDRAM controller:

- vmem_200_512

2. The following minor features are new in **V10**:

- The 3-pt filter is always ON.
- The baseline is determined only by the **R** channel
- The baseline of the signal after the inversion is now equal to 8 ADC units (instead of 0 in V9), which allows correct integral calculation in case the minor signal noise is below the baseline. This shift is taken into account in all parameter calculation algorithms.
- The CFD threshold is programmable to 1/2 or 1/4 of the amplitude
- The direct data readout from channel FIFOs is removed and the data is always stored in the SDRAM memory in all modes.

3. Instead of old pure waveform modes the 'JET' mode introduced which allows to store long wave forms with prehistory of the signal. New Dly register controls the waveform length as well as the length of the prehistory record.

4. The format of the 'AT' and 'ALL' modes data is the same as in **V9**.
5. Both timing parameters of the signal are defined using new algorithms:
 - The CFD time is now defined as the exact moment of crossing of the CFD threshold by a line, connecting the average of the first three points above the threshold with the average of the last three points below the threshold.
 - The Intg time, or the average leading edge time, is defined by integrating the signal from the beginning of the bunch period to the maximum of the signal and then normalizing this integral by the amplitude value.
 - Both algorithms showed best results with certain pulser waveform shapes, but appeared to work not so good with too short leading edges.
6. The integral is now calculated taking into account the baseline shift of 8 ADC units. So the integral should not depend on the signal time in **V10** because there is no negative noise cutoffs.
7. Signal amplitude, naturally, is defined relative to the same 8 ADC units shift.